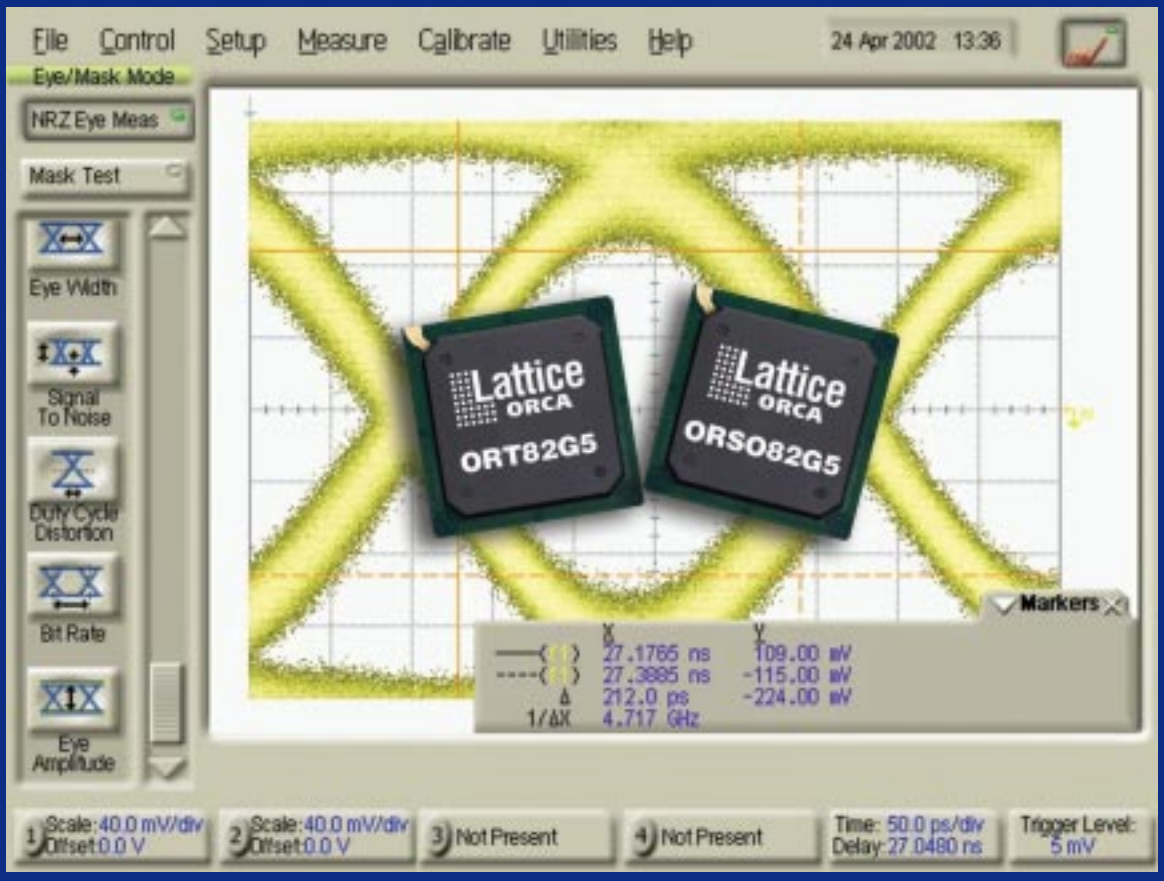
L A T T I C E S E M I C O N D U C T O R

SERDES Handbook

April 2003



Lattice Semiconductor Corporation

Dear Valued Customer,

Lattice Semiconductor is pleased to provide you this second edition of our SERDES Handbook. Since offering the initial version last year, we have introduced several new products based on our superior sysHSI™ technology:

ORT42G5	4 channel version of our leading-edge ORT82G5 FPSC for XAUI and Fibre Channel backplanes
ORSO82G5	8 channels of SERDES running at 2.7 Gbps with embedded SONET capabilities
ORSO42G5	4 channel version of the ORSO82G5
ispGDX2	4 to 20 channels of SERDES running at 850 Mbps with embedded digital switch
ispXPGA™	4 to 16 channels of SERDES running at 850 Mbps with up to 1M gates of non-volatile, reconfigurable FPGA Logic

The content of this Handbook demonstrates Lattice's philosophy of "Bringing the Best Together" through the exceptional capabilities of the world's fastest and most cost-effective programmable backplane devices. Illustrating this concept, the ORT82G5 Field-Programmable System-on-a-Chip (FPSC) includes backplane transceivers supporting eight channels at up to 3.7 Gbits/s coupled with over 10,000 lookup tables (LUTs) based on our ORCA® FPGA architecture.

The ORT82G5 offers the world's finest programmable SERDES with unsurpassed performance:

Programmable Data Rates	• 8 channels at 1.0 to 3.125 Gbps • **Demonstrated performance at up to 3.7 Gbps**
Standards Compliance	• Exceeds XAUI signal integrity specification by at least 50% • Fibre Channel (1G, 2G) and FC-XAUI (10G)
Rx Jitter Tolerance	• 0.75UI superior to XAUI and Fibre Channel specifications
Tx Total Jitter	• 0.17UI superior to XAUI and Fibre Channel specifications
Low Power per SERDES Channel	• <225 mW worst case, including I/O buffers
Fast Locking Times	• Bit Realignment 300 nanoseconds (938 bit times @ 3.125 Gbps)
Transmitter Output (CML)	• Full-amplitude mode: 0.8V p-p Minimum • Half-amplitude mode: 0.4V p-p Minimum
Demonstrated Data Bandwidth	• 3.7 Gbps[1]
Demonstrated Drive Length	• At least 40 inches of FR-4 backplane at 3.125 Gbps[2]

This Handbook contains a variety of updated resources that illustrate the capabilities of all our SERDES-based products, an essential building block for your next system design. We have included:

- Product briefs discussing all of our SERDES-based products
- A product brief describing our 10GbE XGXS intellectual property core which provides a complete bridging solution between XGMII and XAUI for fast design of 10GbE applications.
- Technical notes that provide detailed technical back-up supporting the superiority of Lattice's SEDES-based products:
  - ORT82G5 High-Speed Backplane Measurements
  - High-Speed PCB Design Considerations
  - FPSC SERDES CML Buffer Interface
  - SERDES Test Chip Jitter
  - Lock Times for the ORT82G5 SERDES
  - SERDES Reference Clock
  - Introduction to the sysHSI Block / ispXPGA and ispGDX2

Please contact us should you require additional information on any of our SERDES-based products. We would be pleased to work with you to create world-class communications solutions.

Regards,

Stan Kopec,
Vice President of Corporate Marketing
Lattice Semiconductor

[1] SERDES tested at 3.7 Gbps across 26 inches of FR-4
[2] Running at 3.125 Gbits/sec. SERDES was not tested to failure

SERDES Handbook

Lattice Semiconductor Corporation

Bringing the Best Together

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sysHSI SERDES Technology

Proven SERDES Leadership

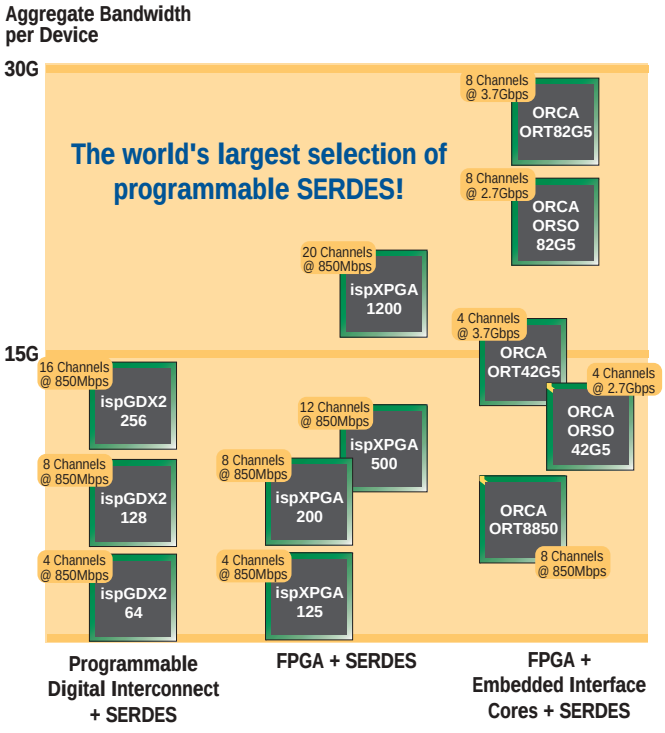
Over the last several years designers have been challenged to obtain higher data rates, reduce PCB traces, reduce connectors, and reduce EMI emissions and susceptibility. SERDES technologies have become increasingly popular as a method to meet these challenges for chip-to-chip, board-to-board, and backplane applications.

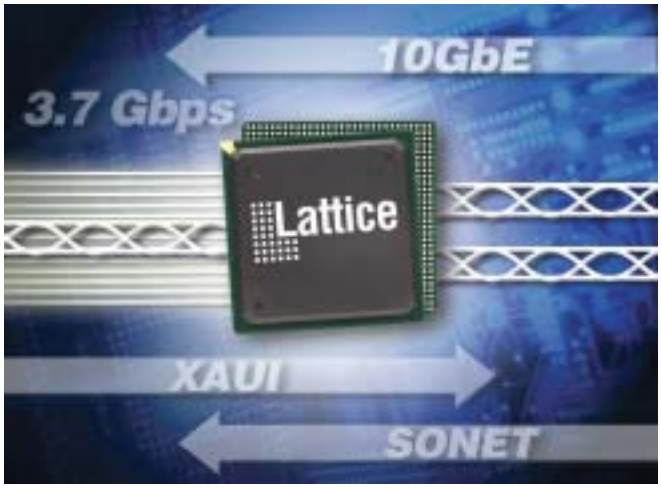
> "FPSC technology allowed NEC to place our custom backplane interface design in the programmable portion of the device, while utilizing the built-in SERDES channels provided in the embedded core of the ORT8850. Lattice FPSCs provide a distinct advantage over a discrete SERDES and FPGA solution."
>
> Shigeki Suyama, General Manager
> **NEC Corporation**

Lattice has implemented sysHSI™ SERDES technologies in a variety of programmable products. High performance SERDES are integrated into Lattice's Field Programmable System Chip (FPSC) devices. A cost effective SERDES is implemented in Lattice's ispXPGA™ family of FPGAs and its ispGDX2 programmable interconnect family.

Lattice sysHSI SERDES technology leads the programmable logic industry in terms of maximum bit rate, low TX jitter, RX jitter tolerance and power consumption per channel. With sysHSI SERDES technology, Lattice products demonstrate the fastest bit rates and the longest error-free connections.

Lattice Programmable SERDES





sysHSI SERDES Key Capabilities

- Wide Range of Bandwidth Supported
  - 126 Mbps to 3.7 Gbps
  - Roadmap to 10 Gbps
- Low TX Jitter
  - 0.17UI @ 3.125 Gbps
- Excellent RX Jitter Tolerance
  - 0.75UI @ 3.125 Gbps
- Programmable Pre-emphasis (FPSCs)
  - 0%, 12.5%, 25%
- Robust High Speed
  - Reliable transmission over:
    - 26 inches of FR4 at 3.7 Gbps
    - 40 inches of FR4 at 3.125 Gbps
    - 75 feet of co-axial cable at 622 Mbps
- Low Power CMOS Operation
  - <225 mW per channel at 3.125 Gbps
  - <50 mW per channel at 622 Mbps
- Choice of Programmable Fabric
  - ispGDX® – Programmable digital interconnect
  - ispXPGA – FPGA
  - FPSC – FPGA + embedded interface core
- Support For Multiple Standards
  - XAUI, Fibre channel, Gigabit Ethernet, SONET

> "Lattice's ORSO82G5 FPSC technology allows our Zeus™ grooming switch to seamlessly interface with existing and emerging SONET line cards, thus preserving the carrier's enormous investment made in SONET-based systems."
>
> Bill Woodruff, VP of Marketing
> **Velio Communication**

SERDES Solutions

High Performance SERDES Solutions

Lattice has integrated high performance SERDES into five of its ORCA® FPSC (Field Programmable System Chip) devices for use in a variety of communications applications. Key features of these SERDES include:

- High bit rates up to 3.7 Gbps
- TX jitter as low as 0.17UI at 3.125 Gbps
- RX jitter tolerance up to 0.75UI at 3.125 Gbps
- Power per channel ≤ 225 mW at 3.125 Gbps

Lattice's high performance SERDES is available on the ORT82G5, ORT42G5, ORSO82G5, ORSO42G5, and ORT8850 FPSC devices.

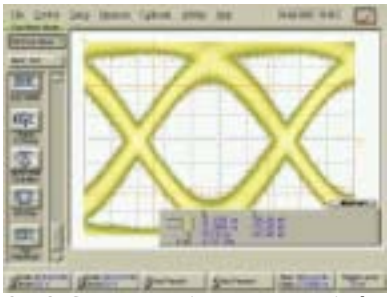
Interoperability

Designers may successfully use Lattice's sysHSI SERDES in conjunction with a variety of other SERDES implemented in a standard chip or ASIC. To date, interoperability has been demonstrated between Lattice SERDES and devices from Velio, AMCC and Agere.

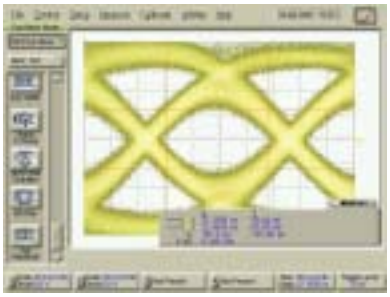
Typical SERDES evaluation test setup for Lattice devices.

Superior SERDES Performance

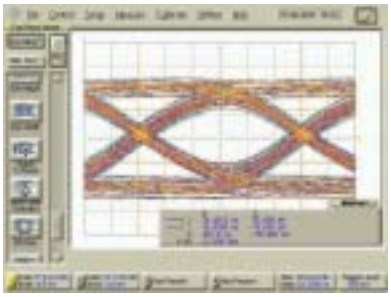
Lattice sysHSI SERDES technology leads the programmable logic industry in terms of maximum bit rate and low jitter. The following actual eye diagrams illustrate the outstanding characteristics of Lattice's sysHSI SERDES technology.



ORT82G5 RX Eye Diagram over 26 inches (65 centimeters) of FR4 at 3.7 Gbps



ORT82G5 RX Eye Diagram over 40 inches (100 centimeters) of FR4 at 3.125 Gbps



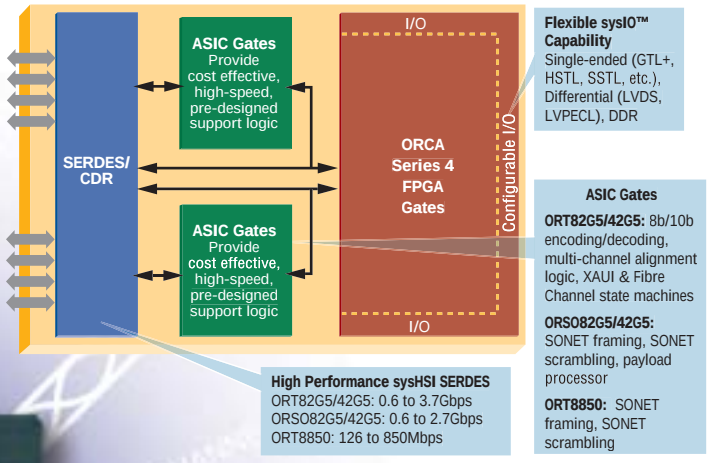
ORSO82G5 RX Eye Diagram over 30 inches (75 centimeters) of FR4 at 2.7 Gbps

ORT82G5/42G5 FPGAs with Embedded Core

3.7 Gbps SERDES + XAUI / Fibre Channel + FPGA

ORT82G5 and ORT42G5 devices provide eight or four high performance SERDES, respectively. Standard compliance and on-chip link state machines make these devices ideal for implementing XAUI, 10 Gbps Ethernet and Fibre Channel links in chip-to-chip and backplane applications.

FPSC Block Diagram



ORSO82G5/42G5 FPGA with Embedded Core

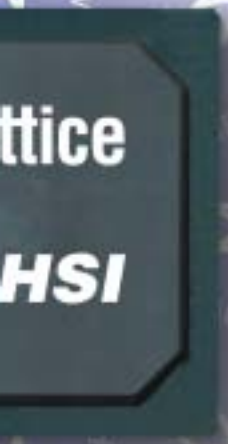
2.7Gbps SERDES + SONET Framing + FPGA

ORSO82G5 and ORSO42G5 devices include eight or four high performance SERDES, respectively. Coupled with on-chip SONET framing, these device provide an excellent SONET-based solution for implementing chip-to-chip or backplane applications.

ORT8850 FPGA with Embedded Core

850Mbps SERDES + SONET Framing + FPGA

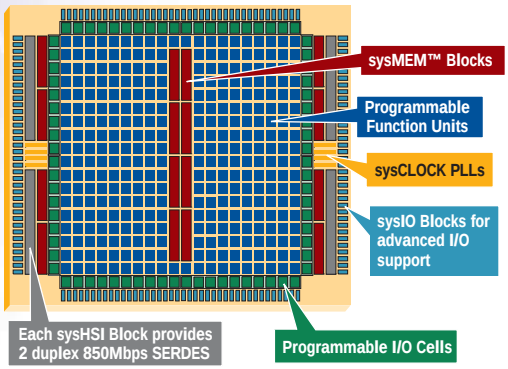
The ORT8850 includes eight 850Mbps SERDES channels plus on-chip SONET framing. The ORT8850 provides an alternative to Ethernet technology for implementing chip-to-chip or backplane applications.



Cost Effective SERDES Soutions

Lattice has developed it's most cost effective SERDES for use in a variety of chip-to-chip, board-to-board, and backplane applications where a moderate speed SERDES is required. This SERDES is available on the ispXPGA and ispGDX2 devices.

ispXPGA Block Diagram

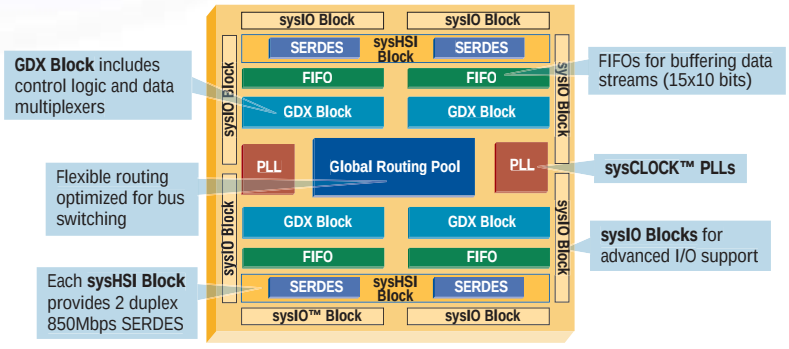


ispXPGA FPGA

Up to 20 x 850 Mbps SERDES + FPGA

The ispXPGA family couples an ispXP™ (ISP™ eXpanded Programmability) based FPGA with up to 20 SERDES channels. With ispXP technology, the ispXPGA family provides infinite reconfigurability through SRAM technology and the benefits of instant-on, security, and a single chip solution through E²CMOS® non-volatility.

ispGDX2 Block Diagram



ispGDX2 – Programmable Interconnect

Up to 16 x 850 Mbps SERDES + Interconnect

The ispGDX2 family provides cost effective SERDES solutions at less than $2.00 per channel for high volume applications. These SERDES are coupled with a multiplexer-based programmable interconnect and switching fabric and flexible I/Os. Many designers use the ispGDX2 device as a universal parallel-to-serial converter.

sysHSI SERDES Enabled Devices

	High Performance SERDES				Cost Effective SERDES	
	ORT82G5 / 42G5	ORSO82G5 / 42G5	ORT8850H	ORT8850L	ispXPGA	ispGDX2
Data Rate per Channel	3.7 – 0.6 Gbps	2.7 – 0.6 Gbps	850 – 126 Mbps	850 – 126 Mbps	850 – 400 Mbps	850 – 400 Mbps
# of Channels	8 / 4	8 / 4	8	8	4 – 20	4 – 16
SERDES I/O	CML	CML	LVDS	LVDS	LVDS	LVDS
TX Jitter	0.17UI	0.16UI	0.25UI	0.25UI	0.25UI	0.25UI
RX Jitter	0.75UI	0.79UI	0.6UI	0.6UI	0.4UI	0.4UI
On-Chip Termination	Yes	Yes	Yes	Yes	No	No
Pre-emphasis Settings	25, 12.5, 0%	25, 12.5, 0%	—	—	—	—
Power / Channel	225 mW	225 mW	50 mW	50 mW	65 mW	65 mW
Encoding Support	8b/10b	SONET	SONET	SONET	10b/12b 8b/10b*	10b/12b 8b/10b*
Standards Support	XAUI, Fibre Channel Gigabit Ethernet	SONET-based SERDES links	SONET-based SERDES links	SONET-based SERDES links	Proprietary SERDES links	Proprietary SERDES links
FPSC Functionality	8b/10b encoding XAUI & Fibre channel link state machines, multi-channel alignment	Pseudo-SONET Framing, TOH insertion/extraction multi-channel alignment, payload cell processor	Pseudo-SONET Framing, TOH insertion/extraction multi-channel alignment, pointer mover	Pseudo-SONET Framing, TOH insertion/extraction multi-channel alignment, pointer mover	—	—
Programmable Section	10,368 LUTS 643K Gates 372 / 204 I/O	10,368 LUTS 643K Gates 372 / 204 I/O	16,192 LUTS 899K Gates 297 I/O	4,992 LUTS 397K Gates 278 I/O	1.9K – 15.3K LUTS 125K – 1.2M Gates 176 – 496 I/O	ispGDX2 multiplexer and interconnect fabric
Typical Programmable Functions	Bridging, proprietary packet processing	Bridging, proprietary packet processing	Bridging, proprietary packet processing	Bridging, proprietary packet processing	PCI, SDRAM interface, Utopia interface	Multiplexer

* Bit alignment. 8b/10b encoding/decoding must be implemented outside of the sysHSI block.

Serial Standards Quick Reference

Specification	Fibre Channel	Infiniband	SFI-5	XAUI	Lattice ORT82G5
Baud Rate	1.0625 Gbps	2.5 Gbps	2.5 Gbps	3.125 Gbps	3.125 Gbps
TX Total Jitter	0.65UI	0.35UI	0.35UI	0.35UI	0.17UI
RX Jitter Tolerance	0.70UI	0.65UI	0.65UI	0.65UI	0.75UI

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3.7 Gbps DEMONSTRATED!

ORT82G5/42G5

The World's Fastest Programmable Backplane Transceivers!

Building Better Backplanes...

Lattice Semiconductor has developed a new generation of Field Programmable System Chips (FPSC) targeted at high-speed serial backplane data transmission. Built on the ORCA® Series 4 reconfigurable embedded system-on-a-chip (SoC) architecture, the ORT82G5 contains eight backplane transceiver channels, each operating in the range from 600 Mbits/sec to 3.7 Gbps, together with a full-duplex synchronous interface with built-in clock and data recovery (CDR), and more than 10,000 lookup tables. The ORT42G5 provides the same functionality with four SERDES channels.

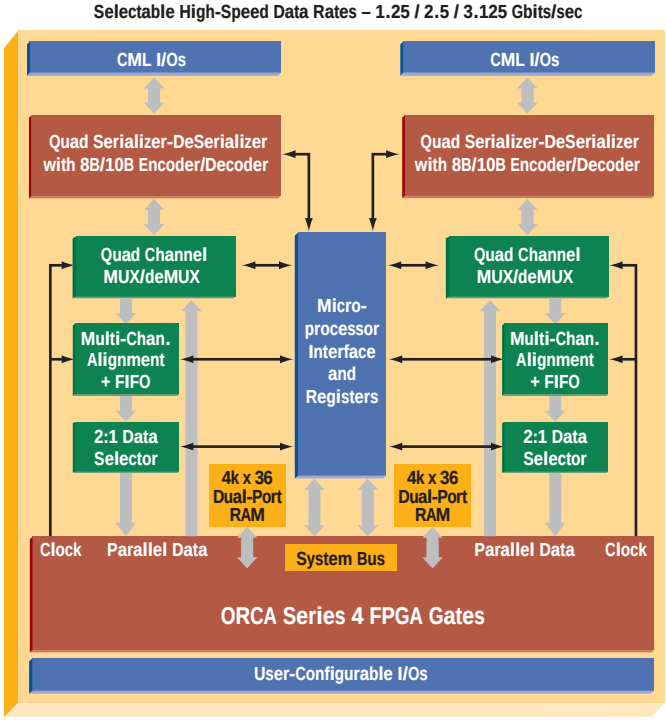
Designers can also use the devices to drive high-speed data transfers across buses within systems because of the embedded 8b/10b capability. For example, with the ORT82G5, designers can build a 20 Gbps bridge (10 Gbps work and 10 Gbps protect) for 10 Gbps Ethernet; the high-speed SERDES interfaces implement two XAUI interfaces with configurable back-end interfaces such as XGMII implemented on the FPGA side. The ORT82G5 can also be used to provide two full 10 Gbps backplane data connections for work and protection between a line card and switch fabric. The ORT42G5 can be used for one full-duplex 10 Gbps backplane data connection between a line card and switch fabric.

Both the ORT82G5 and ORT42G5 offer a clockless high-speed interface for inter-device communication on a board

or across a backplane. The built-in clock recovery of the ORT82G5 and ORT42G5 allows higher system performance, easier-to-design clock domains in a multiboard system, and fewer signals on the backplane.

Network designers will also benefit from the backplane transceivers as network termination devices. The devices support embedded 8b/10b encoding/decoding and link state machines for 10G Ethernet, as well as Fibre Channel.

ORCA ORT82G5 Block Diagram



Note: The ORT42G5 provides one quad SERDES channel.

Key Features and Benefits

- High Performance ORCA Series 4 FPGA Gates:
  - Internal performance of > 250 MHz.
  - Over 10,000 Lookup Tables.
  - 1.5V operation (30% less power than 1.8V operation)
  - Comprehensive I/O selections including LVTTL, LVCMOS, GTL, GTL+, PECL, SSTL3/2, HSTL, ZBT, DDR, LVDS, bus-LVDS, and LVPECL.
- Ease of Design
  - Supported by ispLEVER™ ver. 3.0 design software.
  - Complete ORT82G5 and ORT42G5 design kits supplies simulation models for embedded core, configuration tool, and integrates with ispLEVER ver. 3.0 design software.
- Easy System Integration
  - SERDES performance exceeds XAUI specifications.
  - XGMII IP core for FPGA side supports interfacing to 10 Gbps Ethernet MACs.
  - XAUI to XGMII translator (XGXS IP Core)
  - Easy integration of 10 Gbps Ethernet and Fibre-Channel for data over fibre applications.

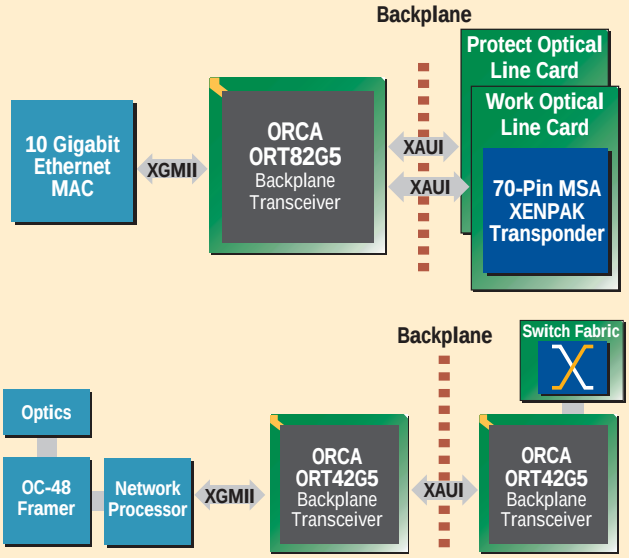
ORCA ORT82G5 and ORT42G5 Attributes

Device	FPGA Usable Gates	PFUs	LUTs	Registers	PFU RAM Bits	EBR RAM Bits	FPGA User I/O	Package	FPGA I/O Compatibility	SERDES Channels	Max Data Rate per Channel
ORT82G5	333 - 643K	1,296	10,368	12,780	277K	111K	372	680PBGAM	1.5/1.8/2.5/3.3V	8	3.7 Gbps
ORT42G5	333 - 643K	1,296	10,368	12,780	277K	111K	204	484PBGAM	1.5/1.8/2.5/3.3V	4	3.7 Gbps

ORCA ORT82G5 and ORT42G5 Applications

The ORT82G5 and ORT42G5 are ideal for 10 Gigabit Ethernet systems. The ORT82G5 provides 8 channels of 3.125 Gbps data to drive across two XAUI backplanes for work and protection. The ORT42G5 provides one channel of 3.125 Gbps data to drive across one XAUI backplane connection. Both devices connects directly to a XENPAK optical transponder on the line card side, and to a 10 GbE MAC via an XGMII interface implemented in FPGA gates. This elegant solution allows network system designers to immediately deploy 10 GbE in the LAN, in the MAN, and in the WAN.

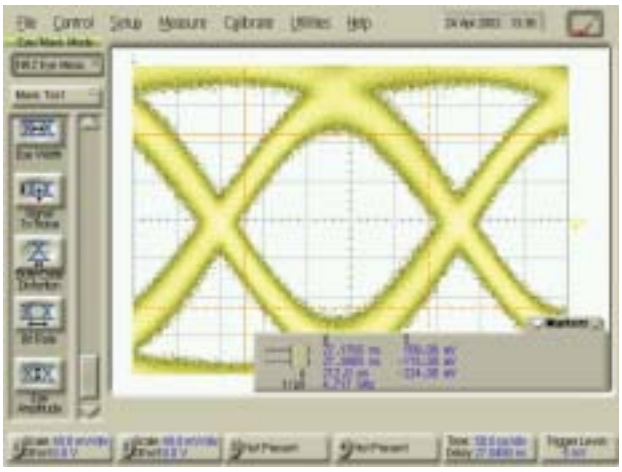
The ORT42G5 can be used as a cost-effective backplane driver for systems requiring up to 10Gbps across a XAUI-based backplane. The programmable gates on the ORT42G5 are ideal for implementing interfaces to switch fabrics or network processors.



Embedded Core Features

- Robust High Speed - Reliable transmission over:
  – 26 inches of FR4 at 3.7 Gbps
  – 40 inches of FR4 at 3.125 Gbps
  – 75 feet of co-axial cable at 622 Mbps
- Lowest power consumption of any programmable SERDES – less than 225mW (worst case) per channel at 3.125 Gbps over full temperature/voltage range.
- Low Tx Jitter: 0.17UI @ 3.125 Gbps
- Excellent Receive Jitter Tolerance: 0.75 UI @ 3.125 Gbps
- Transmit pre-emphasis (programmable) for improved receive data eye opening: 0%, 12.5%, 25%
- 32-bit (8b/10b) or 40-bit (raw data) parallel internal bus for data processing in FPGA logic.
- Exceeds XAUI serial data specification for 10 GbE applications with protection. Includes integrated XAUI state machine.
- Compliant to Fibre Channel physical layer specification, including integrated Fibre Channel state machine.
- SERDES has low-power CML buffers to allow use with optical transceiver, coaxial copper media, shielded twisted pair wiring or high-speed backplanes such as FR-4.

ORT82G5 and ORT42G5 CDR Eye Diagram Measurements



Actual data eye at 3.7 Gbps across 26 inches of FR-4 backplane with 25% pre-emphasis.

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www.latticesemi.com

ORSO82G5/42G5

High Speed — Low Overhead — Serial SONET Backplane Transceiver

Building Better Backplanes...

Lattice Semiconductor has developed a next-generation Field Programmable System-on-a-Chip (FPSC) solution for high-speed serial SONET backplane data transmission. Built on the ORCA® Series 4 reconfigurable embedded system on-a-chip (SoC) architecture, the ORSO82G5 includes eight backplane transceiver channels, each operating at up to 2.7 Gbps data rate, providing a full-duplex synchronous interface with built-in Clock/Data Recovery (CDR) and over 10,000 lookup tables. The ORSO42G5 provides the same functionality with four SERDES channels.

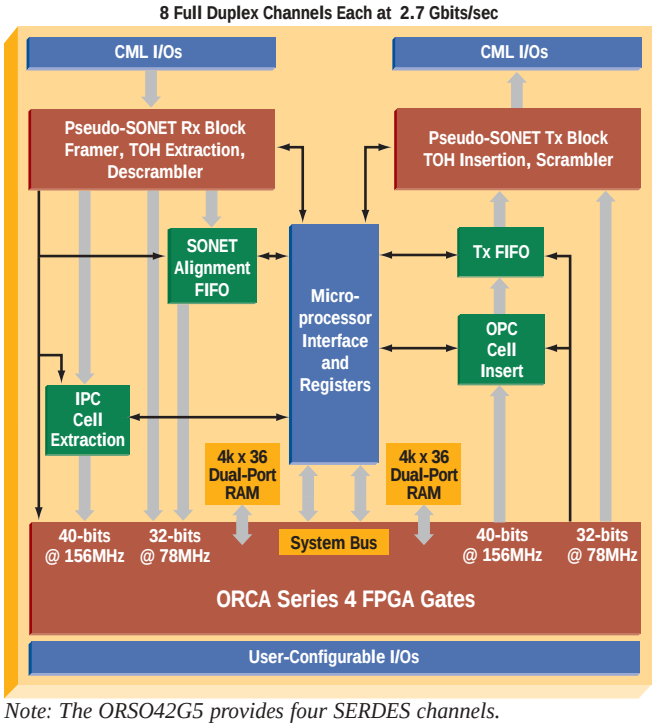
The ORSO82G5 provides a full 10 Gbps backplane data connection with protection between a line card/redundant line card and switch fabric/redundant switch fabric. The FPGA portion can be used to implement 2.5 Gbps and 10 Gbps SONET-based switch fabric interfaces. The ORSO42G5 can also implement a 10 Gbps backplane without the protection scheme.

The ORSO82G5 and ORSO42G5 provide a SERDES-based high-speed interface for inter-device communication on a board or across a backplane. The built-in clock recovery of the ORSO82G5 and ORSO42G5 supports higher system performance, easier-to-design clock domains in a multiboard system, and fewer signals on the backplane.

The ORSO82G5 and ORSO42G5 support SONET data scrambling and descrambling, streamlined SONET framing, transport overhead handling, cell insertion and extraction, idle cell insertion/deletion plus the programmable logic to

terminate the network into proprietary systems. All SONET functionality is hidden from the user and no prior networking knowledge is required. The user can optionally bypass all SONET functionality (SERDES-only mode) to enable the implementation of proprietary processing schemes. Optional Cell Mode processing blocks provide a glueless interface to switch fabrics, 2.5 Gbps and 10 Gbps network processors, or can be used when both ends of a link are either ORSO82G5 or ORSO42G5 devices for generic cell-based backplanes.

ORCA ORSO82G5 Block Diagram



Note: The ORSO42G5 provides four SERDES channels.

Key Features and Benefits

- High Performance ORCA Series 4 FPGA Gates:
  - Internal performance of > 250 MHz.
  - Over 10,000 lookup tables.
  - 1.5V operation (30% less power than 1.8V operation)
  - Comprehensive I/O selections including LVTTL, LVCMOS, GTL, GTL+, PECL, SSTL3/2, HSTL, ZBT, DDR, LVDS, bus-LVDS, and LVPECL.
- Ease of Design
  - Supported by ispLEVER™ ver. 3.0 design software.
  - Complete ORSO82G5 and ORSO42G5 design kits supplies simulation models for embedded core, configuration tool, and ispLEVER ver. 3.0 design software integration.
- Easy System Integration
  - Programmable platform for bridging network processor/routing devices to switch fabrics over SONET SERDES. On the line side, the ORSO82G5 can be utilized to provide a flexible interface to various optical modules (such as VSR-3).

ORCA ORSO82G5 and ORSO42G5 Attributes

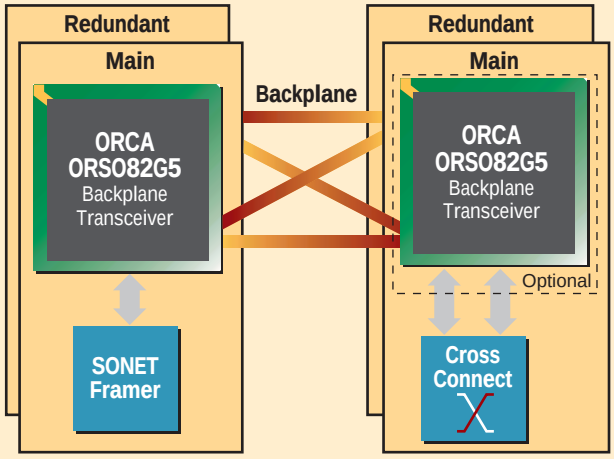
Device	FPGA Usable Gates	PFUs	LUTs	Registers	PFU RAM Bits	EBR RAM Bits	FPGA User I/O	Package	FPGA I/O Compatibility	SERDES Channels	Max Data Rate per Channel
ORSO82G5	333 - 643K	1,296	10,368	12,780	277K	111K	372	680PBGAM	1.5/1.8/2.5/3.3V	8	2.7 Gbps
ORSO42G5	333 - 643K	1,296	10,368	12,780	277K	111K	204	484PBGAM	1.5/1.8/2.5/3.3V	4	2.7 Gbps

Embedded Core Features

- FIFOs optionally align incoming data across groups of two or four channels. The ORSO82G5 can also align across 8 channels.
- In-band management through transport overhead insertion and extraction. Options to insert SONET TOH bytes or have them automatically inserted with default values.
- Programmable enable of SONET scrambler/descrambler.
- Two 4K x 36 dual-port RAMs with access to the programmable logic.
- Optional bypass of SONET frames for raw data interface to the FPGA logic.
- Optional Cell Mode available that uses SONET for physical layer and cells inserted as payload.
- Multiple fixed-length cell payload sizes available (64, 68, 72 or 80 bytes).
- Cell generation and insertion into payload on Tx.
- Cell extraction and error checking on Rx.
- Automatic idle cell generation and deletion for rate matching
- No knowledge of SONET/SDH needed in generic applications. Simply supply data (125 MHz – 168.75 MHz clock) and an optional frame pulse.
- The ORSO82G5 provides an embedded eight-channel HSI core running at 2.7 Gbps serial bandwidth per channel for a total chip bandwidth of >20 Gbps (full duplex).
- The ORSO42G5 provides an embedded four-channel HSI core running at 2.7 Gbps serial bandwidth per channel >10 Gbps bandwidth (full duplex).
- Error-free operation demonstrated at 2.7 Gbps across 40” of FR-4 backplane and two connectors.
- Transmit pre-emphasis (programmable) for improved receive data eye opening.
- High-speed SERDES programmable serial data rates from 600 Mbits/s to 2.7 Gbps.

ORCA ORSO82G5 Application – Backplane Driver for Grooming Switch

The ORSO82G5 FPSC is ideal for driving backplanes in SONET-based systems. The device provides 8 channels of 2.7 Gbits/s serial bandwidth to drive across the backplane. The programmable gates on the ORSO82G5 allow for flexible interfaces to the framer and cross-connect devices. The ORSO42G5 provides the same capability, however without redundancy.



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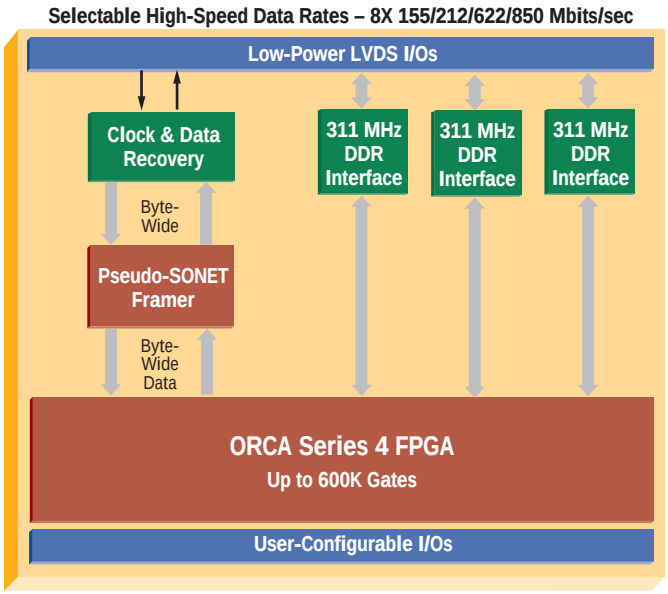
ORCA ORT8850

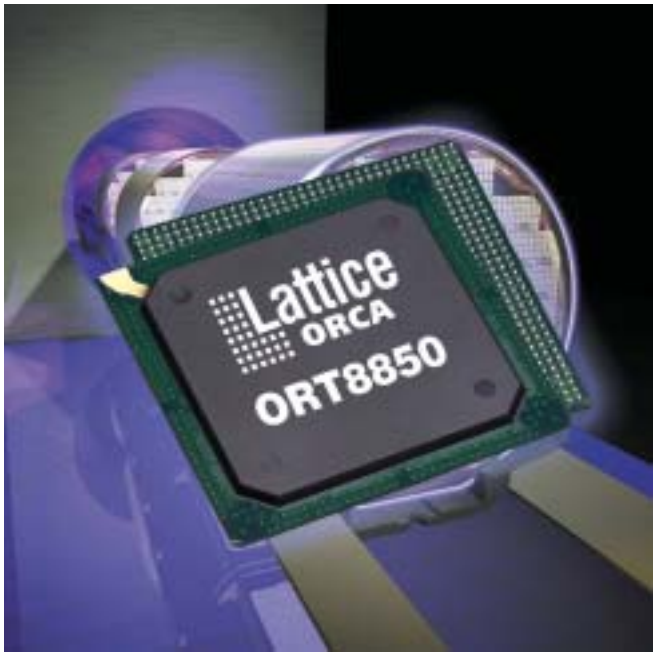
8-Channel High-Speed Serial Backplane Driver

Lattice has developed a solution for designers who need the many advantages of FPGA-based design implementation, coupled with high-speed serial backplane data transfer. Built on the ORCA® Series 4 reconfigurable embedded system-on-a-chip (SoC) architecture, the ORT8850 family is made up of backplane transceivers containing eight channels, each operating at up to 850 Mbits/s (6.8 Gbits/s when all eight channels are used) full-duplex synchronous interface, with built-in clock and data recovery (CDR) in standard-cell logic, along with up to 600K usable FPGA system gates.

The ORT8850 family offers a clockless high-speed interface for inter-device communication, on a board or across a backplane. The built-in clock recovery of the ORT8850 allows higher system performance, easier- to-design clock domains in a multiboard system, and fewer signals on the backplane. Network designers will also benefit from the backplane transceiver as a network termination device. The backplane transceiver offers SONET scrambling/descrambling of data and streamlined SONET framing, pointer moving, and transport overhead handling, plus the programmable logic to terminate the network into proprietary systems. For non-SONET applications, all SONET functionality is hidden from the user and no prior networking knowledge is required.

ORCA ORT8850 Block Diagram





Also included on the device are three full-duplex, high-speed parallel interfaces, consisting of 8-bit data, control (such as start-of-cell), and clock. The interface delivers double data rate (DDR) data at rates up to 311 MHz (622 Mbits/s per pin), and converts this data internal to the device into 32-bit wide data running at half rate on one clock edge. Functions such as centering the transmit clock in the transmit data eye are done automatically by the interface. Applications delivered by this interface include a parallel backplane interface similar to the RapidIO packet-based interface.

Key Features and Benefits

- High Performance ORCA Series 4 FPGA Gates:
  - Internal performance of > 250 MHz.
  - Up to 600K usable system gates (with ORT8850H).
  - 1.5 V operation (30% less power than 1.8 V operation)
  - Comprehensive I/O selections including LVTTL, LVCMOS, GTL, GTL+, PECL, SSTL3/2, HSTL, ZBT, DDR, LVDS, bused-LVDS, and LVPECL.
- Ease of Design
  - Supported by ORCA Foundry 2001 design software
  - Complete ORT8850 design kit supplies simulation models for embedded core, configuration tool, and integrates with ORCA Foundry 2001

ORCA ORT8850 Attributes

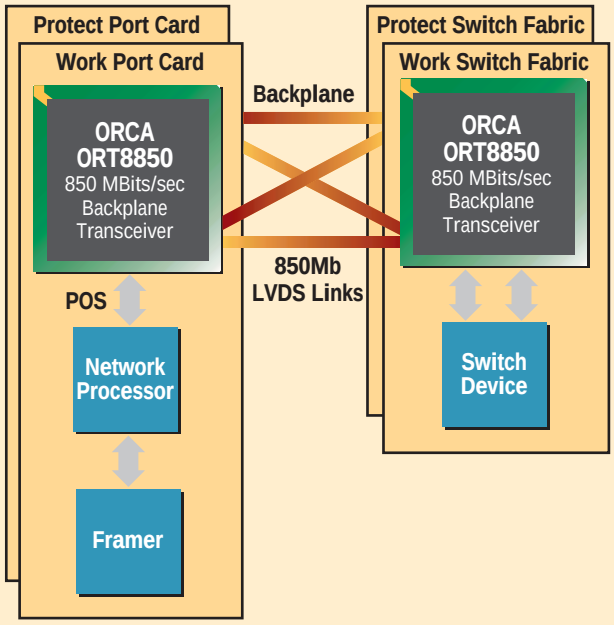
Device	Usable Gates	PFUs	LUTs	Registers	PFU RAM Bits	EBR RAM Bits	Available User I/O 352PBGA	Available User I/O 680PBGAM	I/O Compatibility	PLLs	SERDES Channels	Maximum Data Rate
ORT8850L	360-470K	624	4,992	6,504	154K	74K	161	278	1.8 / 2.5 / 3.3V	4	8	850 Mbits/sec
ORT8850H	530-600K	2,024	16,192	19,824	406K	147K	N/A	297	1.8 / 2.5 / 3.3V	4	8	850 Mbits/sec

Key Features and Benefits (cont.)

- Easy System Integration
  - Supports wide range of SONET-based backplane applications as well as generic data moving for high-speed backplane data transfer. No knowledge of SONET/SDH needed in generic applications: simply supply data, 63 MHz-106 MHz clock, and a frame pulse.
  - High-speed interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
  - Eight-channel HSI function provides 850 Mbits/s serial interface per channel for a total chip bandwidth of 6.8 Gbits/s (full duplex). Rates from 126 Mbits/s to 850 Mbits/s are supported directly (lower rates directly supported through decimation and interpolation).
  - Powerdown option of HSI receiver on a per-channel basis.
  - SONET scrambler/descrambler.
  - Three full-duplex, double data rate (DDR) I/O groups include 8-bit data, one control, and one clock. Each interface is implemented with LVDS I/Os that include on-board termination to allow long-haul driving of backplanes, such as those similar to the industry standard RapidIO interface.
  - Redundant outputs and multiplexed redundant inputs for CDR I/Os allow implementation of eight channels with redundancy on a single device.
  - On-chip, phase-lock loop (PLL) clock meets B jitter tolerance specification of ITU-T recommendation G.958.
  - FIFOs align incoming data across all eight channels (two groups of four channels or four groups of two channels). Optional ability to bypass alignment FIFOs.
  - 1 + 1 protection supports STS-12/STS-48 redundancy by either software or hardware control for protection switching applications. STS-192 and above rates are supported through multiple devices.

ORT8850 Application – 4 Gbits/sec Serial Backplane for Switching

- SERDES operates at up to 850 Mbits/sec. With one ORT8850 on port-card and one on switch-card, 4 Gbits/sec throughput achieved
- 850 Mbits/sec with SONET scrambling (3.3% overhead) allows > 800 Mbits/sec raw data transfer
- Packet-Over-SONET (POS) or RapidIO-like interface to Network Processor on port card



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ispXPGA

Non-Volatile Infinitely-Reconfigurable Instant-On FPGAs

The World's First FPGA to Offer Non-Volatility and Reconfigurability

The ispXPGA™ family of devices allows the creation of high-performance logic designs that are both non-volatile and infinitely re-configurable. Other FPGA solutions force a compromise, being either re-programmable, or reconfigurable, or non-volatile. This family offers *all* of these capabilities with a mainstream architecture containing the features required for today's system-level design. We call this concept ispXP™, for eXpanded Programmability.

ispXPGA Programming / Configuration

- Auto-configure at Power-up in Microseconds
- Reconfigure In-System
- Reprogram During System Operation
- Configure from On-Chip E^2 or CPU
- Set Security Bits to Prevent Readback
- No External Configuration Memory
- Totally Secure from Bit-Stream Snooping

Key Features and Benefits

- Non-Volatile, Infinitely Reconfigurable
  - Power-up in Microseconds via On-Chip E^2 Cells for Instant-on Usage
  - Reconfigure SRAM-based Logic In-System
  - In-System Programmable
  - No External Configuration Memory
- System-Level Integration
  - 139K to 1.25M System Gates
  - Up to 496 I/Os
  - Up to 414Kb Embedded Memory
- High Performance Logic Blocks (PFUs)
- Block and Distributed Memory
- Variable-Length-Interconnect™ Routing
- sysCLOCK™ PLLs for Clock Management
- sysIO™ for High Performance Interfacing
- sysHSI™ for 850Mbps Serial Communications
- 1.8V, 2.5V, and 3.3V Operation

Instant-on
Non-Volatile &
Reprogrammable

ispXPGA Family

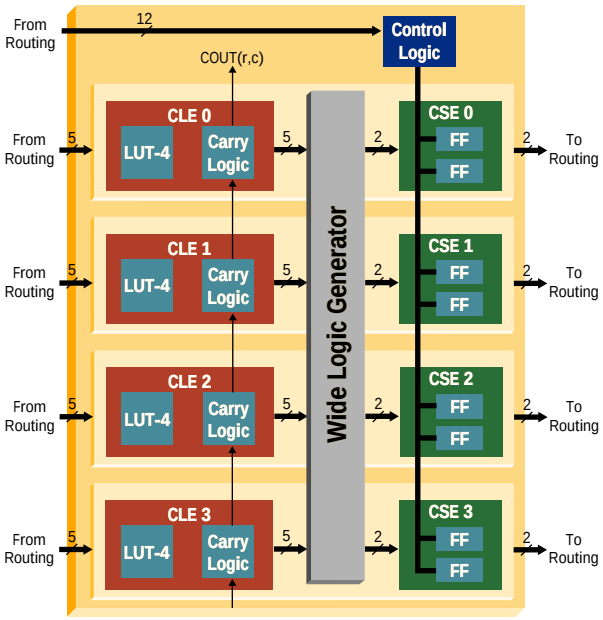
Family Member	System Gates	PFUs	LUT-4	Logic FFs	Block RAM	Distributed RAM	sysHSI™ Channels	User I/O	Vcc	Packaging	Body Size
ispXPGA 125	139K	484	1936	3.8K	92K	30K	4	160 176	1.8, 2.5, 3.3V	256 fpBGA 516 fpBGA*	17x17mm 31x31mm
ispXPGA 200	210K	676	2704	5.4K	111K	43K	8	160 208	1.8, 2.5, 3.3V	256 fpBGA 516 fpBGA*	17x17mm 31x31mm
ispXPGA 500	476K	1764	7056	14.1K	184K	112K	12	336 336	1.8, 2.5, 3.3V	516 fpBGA* 900 fpBGA	31x31mm 31x31mm
ispXPGA 1200	1.25M	3844	15376	30.8K	414K	246K	20	496 496	1.8, 2.5, 3.3V	680 fpSBGA* 900 fpBGA	40x40mm 31x31mm

* Thermally enhanced

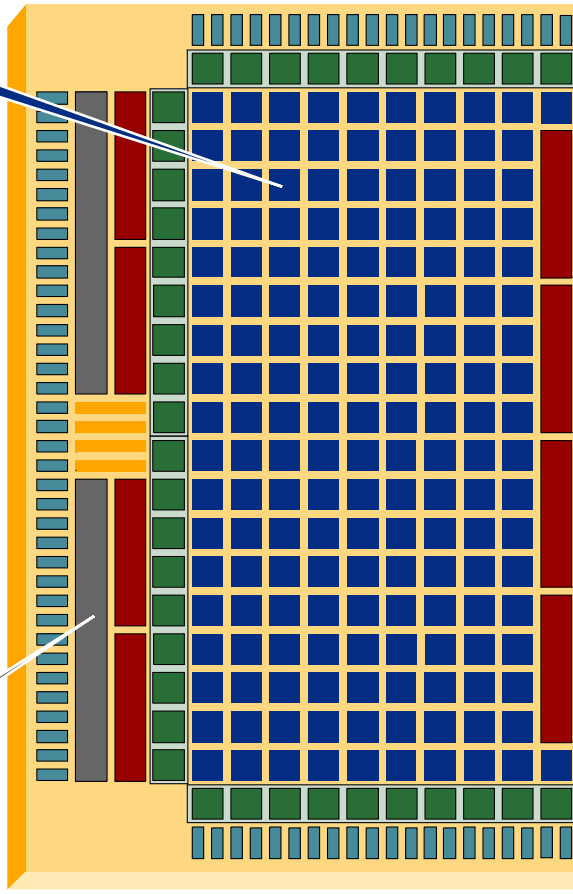
ispXPGA Architecture

Programmable Function Unit (PFU)

- Dedicated Arithmetic Logic
- Up to 20-Input Logic Functions
- Dual Flip Flop per LUT-4 for Pipelining
- 64 Bits of Distributed Memory
  - Single-Port, Dual-Port or Shift Register

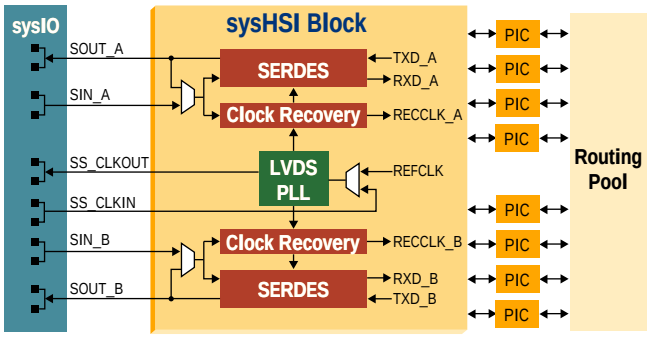


ispXPGA Block Diagram



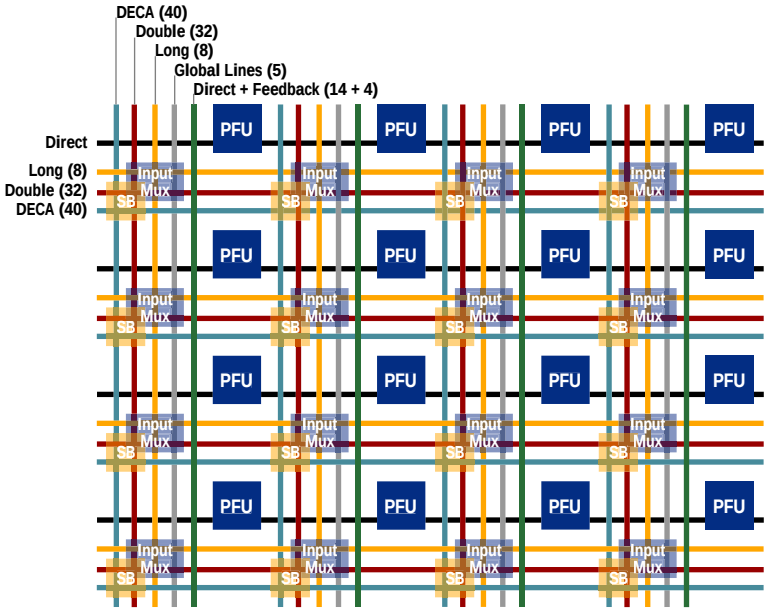
sysHSI Blocks

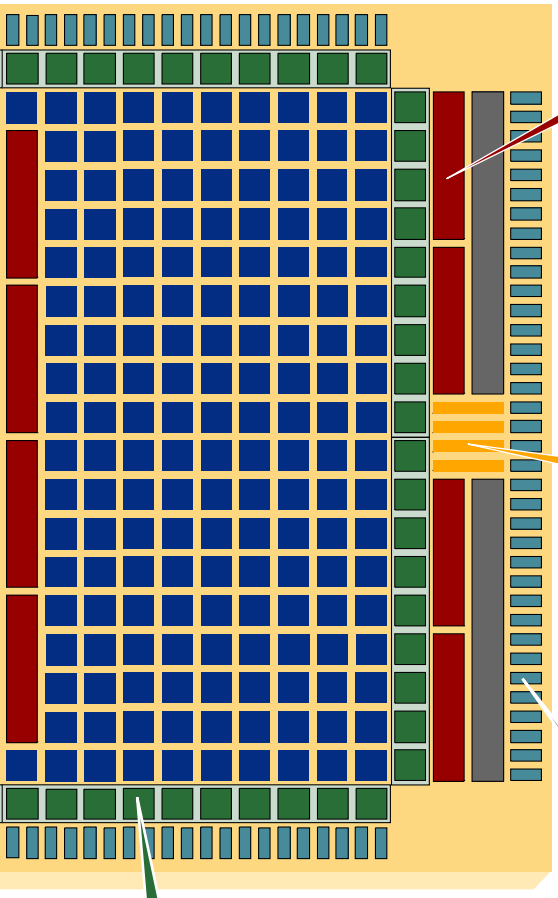
- Dedicated High-Speed Interface (HSI) Circuits
- Built-in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)
- 850 Megabit LVDS, Up to 20 Channels per Device
- Can be utilized separately to allow multiple reference clocks and data rates
- 8B/10B and 10B/12B Coding
- Up to 34 Gbps



Optimized Routing Resources

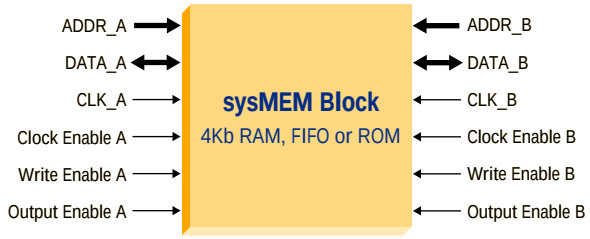
- Segmented Routing for Superior Fitability and Performance
- Intra-PFU Feedback
- Direct, Double, Deca and Long Connects





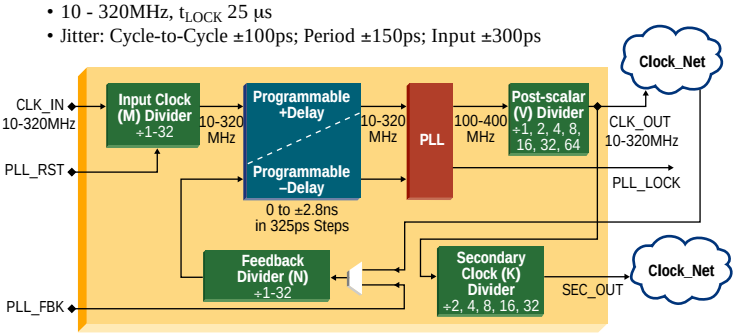
sysMEM™ Embedded RAM Blocks

- Up to 414Kb of Dedicated Memory per ispXPGA
- Configurable as Single- or Dual-Port RAM, FIFO or ROM
- 512x9 Bits or 256x18 Bits
- Cascadable Width and Depth
- Sub-3ns Access Times



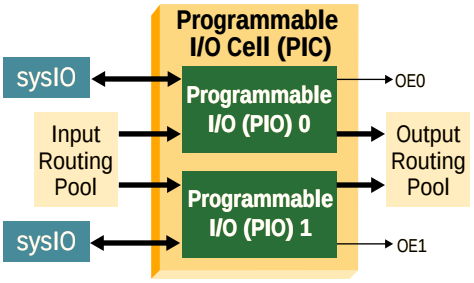
sysCLOCK Phase Locked Loops (PLL)

- 8 PLLs per Device
  - Plus 8 Global Clocks
  - Plus 8 Low-Skew Clock Nets
- Clock Frequency Synthesis
- Multiple Clock Signal Generation
- Device or Board Clock Alignment
- 10 - 320MHz, t_{LOCK} 25 µs
- Jitter: Cycle-to-Cycle ±100ps; Period ±150ps; Input ±300ps



Flexible I/O Cells

- Separate Input, Output and OE Registers
- Flexible Set, Reset, Clock Enable and Polarity
- Input Register Offers Delay Option for Zero t_{HOLD}
- Programmable Output Slew Rate



sysIO High Speed Interface

- Supports Multiple Interface Standards
- Programmable Drive Strength for Series Termination
- Programmable Bus Maintenance
- Multiple Banks for Easy Control

Chip to Memory	Chip to Chip	Chip to Backplane
SSTL2 I and II	LVTTL	PCI33_3
SSTL3 I and II	LVCMOS 3.3	PCI66_3
HSTL I	LVCMOS 2.5	PCI-X
HSTL III	LVCMOS 1.8	GTL+
HSTL IV	Prog. Impedance	AGP
CTT		Bus-LVDS
↓		LVDS
SDRAM		LVPECL
DDR SRAM		
QDR SRAM		
ZBT SRAM		

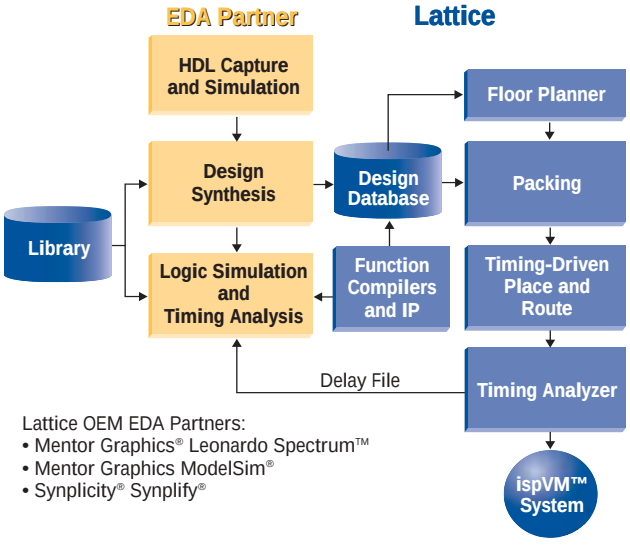
ispLEVER™ Design Software

Lattice's ispLEVER is a new generation of PLD design tool equipped to provide a complete system for FPSC, FPGA, ispXPLD™, CPLD, ispGDX® and SPLD design. ispLEVER includes a fully integrated, push-button design environment and advanced features for interactive design optimization and debug.

Features

- Fully Integrated Synthesis and RTL and Timing Simulation Tools
- Complete Design Flow for All In-System Programmable (ISP™) Lattice Device Families
- Advanced Timing-Driven Placement and Routing
- IP Manager and Module Generator
- Fast, Efficient Run Times and Competitive Device Performance and Utilization
- Supported by Libraries from Leading CAE Vendors
  - Aldec
  - Cadence
  - Innoveda
  - Mentor Graphics
  - Synopsys
  - Synplicity
- Windows® and UNIX® Solutions

ispLEVER Design Software Flow Chart



ispXPGA Select Performance

T_A = 25° C; V_{CC} = 1.8V

Function		Speed
4-Input LUT Delay		440ps
Synchronous Counter	8-bit	334MHz
Loadable Up/Dn Carry-Ripple Counter	64-bit	156MHz
Carry-Ripple Adder	64-bit	232MHz
Multiplexer	64:1	237MHz
De-Multiplexer	1:64	371MHz
Shift Reg Up/Dn, Circular Shift	64-bit	315MHz
Barrel Shifter	64-bit	184MHz
PLL Frequency	Min Max	10 MHz 320 MHz
LVDS with Clock Recovery	Max	850Mbit

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ispGDX2

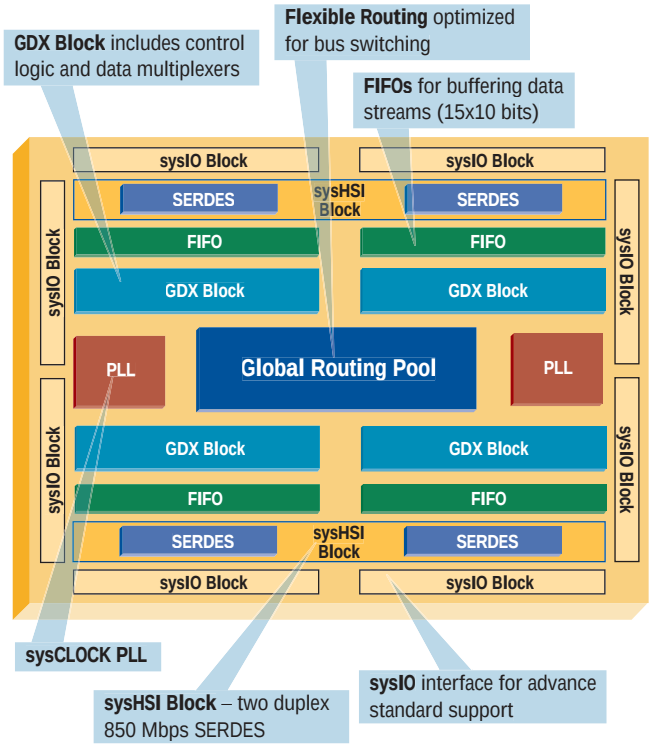
High Performance Digital Crosspoint Switch

Fast Serial I/O and High Bandwidth Bus Interface

The ispGDX2™ family is Lattice's next generation in-system programmable (ISP™) high performance digital crosspoint switch for high-speed bus switching and interfacing with bandwidth of up to 38Gbps. This family combines a flexible switching architecture with advanced high speed serial I/O (sysHSI™ blocks), sysCLOCK™ PLLs, and sysIO™ interfaces to meet the needs of today's high-speed systems. A multiplexer based architecture and on-chip control logic facilitate the high performance implementation of common switching functions.

ispGDX2 devices are provided in 3.3V, 2.5V or 1.8V core voltage versions and can be programmed in-system via an IEEE 1149.1 interface that is compliant with the IEEE 1532 standard. Voltages required for the I/O buffers are independent of the core voltage supply. This further enhances the design flexibility of the family. Typical applications for the ispGDX2 include multi-port multi-processor interfaces, serial backplanes, wide data and address bus multiplexing, programmable control signal routing and programmable bus interfaces.

ispGDX2-64 Block Diagram



Key Features and Benefits

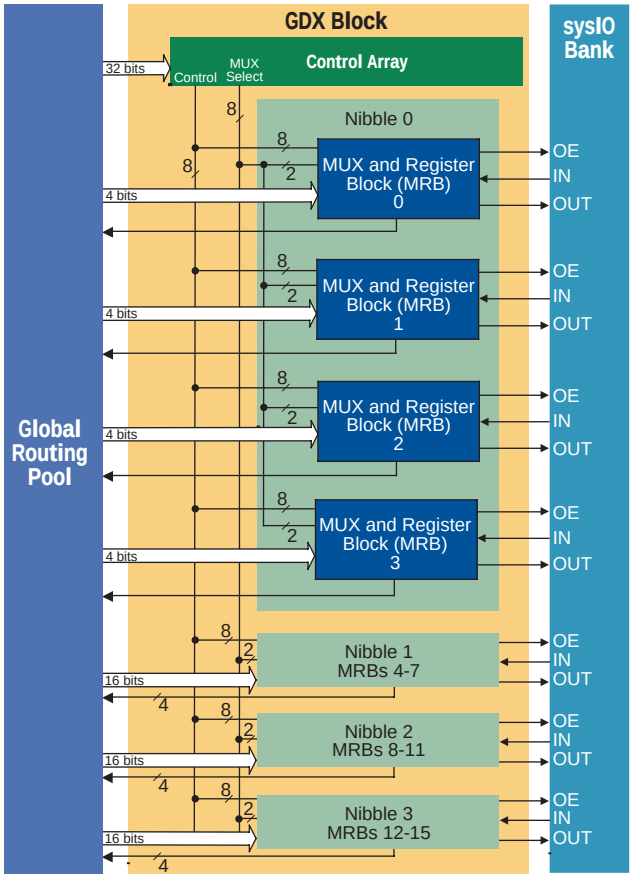
- High Performance Bus Switching
  - 13.6 Gbps (SERDES), 38 Gbps (without SERDES)*
  - Up to 16 (15X10) FIFOs for data buffering
  - High-speed Performance: f_{MAX} = 330 MHz, t_{PD} = 3.0ns
  - I/O intensive: 64 to 256 I/Os
  - Expanded MUX capability up to 188:1 MUX
- sysCLOCK PLL
  - Frequency synthesis and skew management
  - Clock shifting, multiply and divide capability
  - Jitter as low as 150ps
  - Up to four PLLs
- sysIO Interfacing
  - LVCMOS 1.8, 2.5, 3.3 and LVTTL support
  - SSTL 2/3 Class I and II support
  - HSTL Class I, III and IV support
  - GTL+, PCI-X support
  - LVPECL, LVDS and Bus LVDS support
  - Hot socketing
- Up to 16 Channels of 850Mbps sysHSI SERDES
  - Serializer/de-serializer (SERDES) included
  - Built-in Clock Data Recovery (CDR)
  - 10B/12B support
    - Encoding / decoding
    - Sync pattern support
    - Symbol alignment
  - 8B/10B support
    - Sync pattern support
    - Symbol alignment
  - Source synchronous capability
- Flexible Programming & Testing
  - IEEE 1532 compliant ISP
  - Boundary Scan test through IEEE 1149.1 Interface

** Bandwidth assumes 50% of I/Os are inputs and 50% are outputs.*

ispGDX2 Architecture

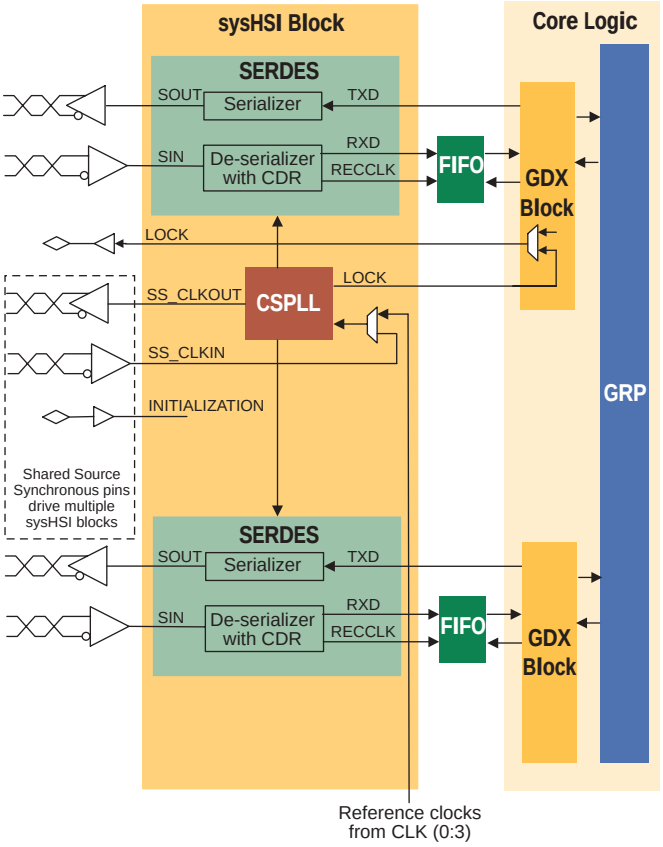
GDX Block

- 4 to 16 GDX Blocks per device
- 16 4:1 MUX and Register Blocks (MRBs) optimized for bus switching
- Separate registers for input, output, and output enable
- 32 input programmable control array provides block-level MUX select, clock, set/reset and output enable



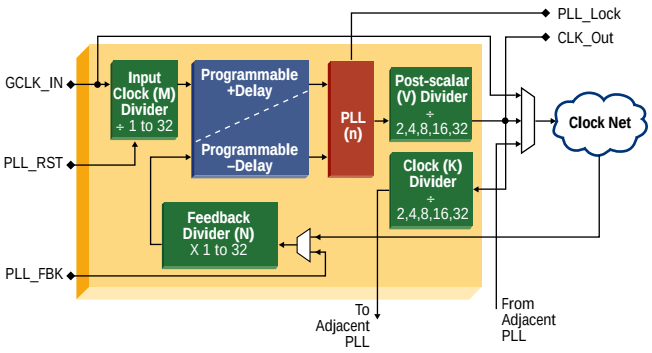
sysHSI – High Speed Interface

- 2 to 8 sysHSI Blocks per device
- Each sysHSI includes two 850 Mbps duplex SERDES (with CDR)
- Multiple sysHSI Blocks can be combined for source synchronous operation



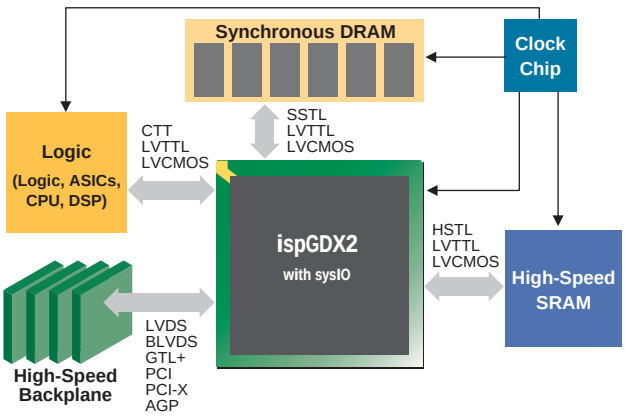
sysCLOCK PLL for Timing Control

- 2 to 4 sysCLOCK PLLs per device
- 10 to 320 MHz PLL operation
- PLL with period jitter of ±150ps



sysIO Interfaces

- On-board sysIO Banks allow ispGDX2 devices to support a wide range of I/O standards
- 8 sysIO Banks per ispGDX2 device
- Each sysIO Bank has its own separate I/O supply voltage and reference voltage

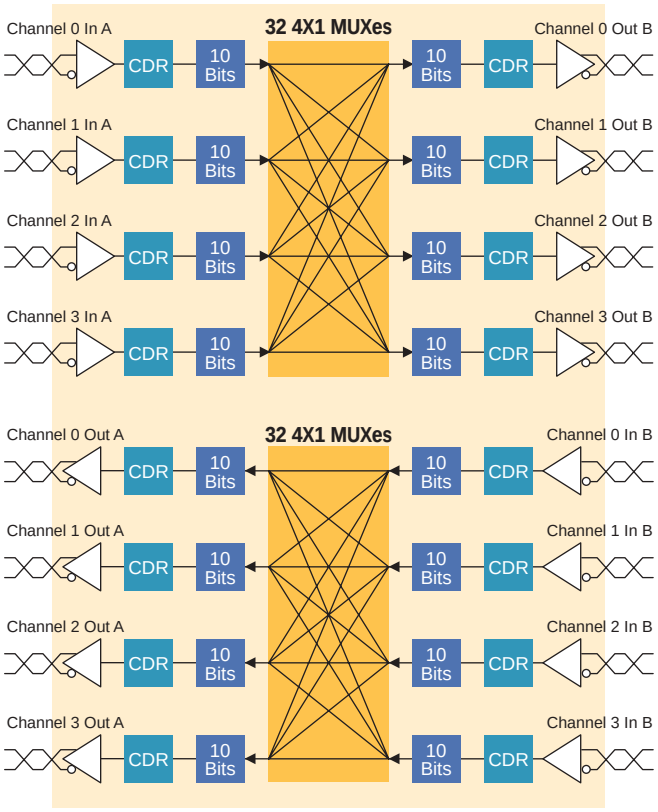


ispGDX2 Applications

4X4 Serial High-Speed Switch

The high performance architecture of the ispGDX2 is perfect for implementing crosspoint switches with multiple devices. In this application, the ispGDX2 device performs:

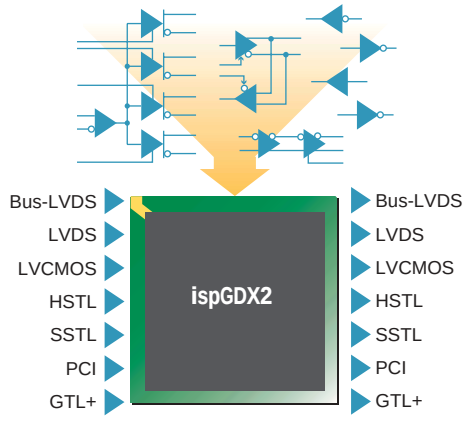
- Bi-directional 4X4 serial high-speed switches
- Bus-LVDS enables bigger crosspoint switches with multiple devices



Flexible I/O Buffer

The ispGDX2 provides a flexible method to integrate multiple buffers into a single device. ispGDX2 devices provide:

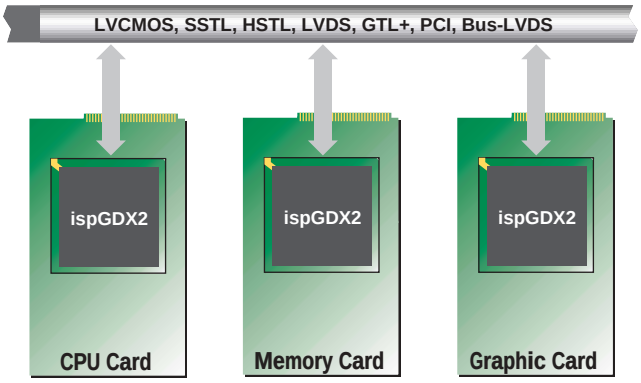
- Support for multiple standards
- In-system programmability and JTAG testability



Flexible High-Speed Backplane Driver

The sysIO capability of the ispGDX2 provides flexility in implementing backplane drivers. In the application below, the ispGDX2 devices provide the following features:

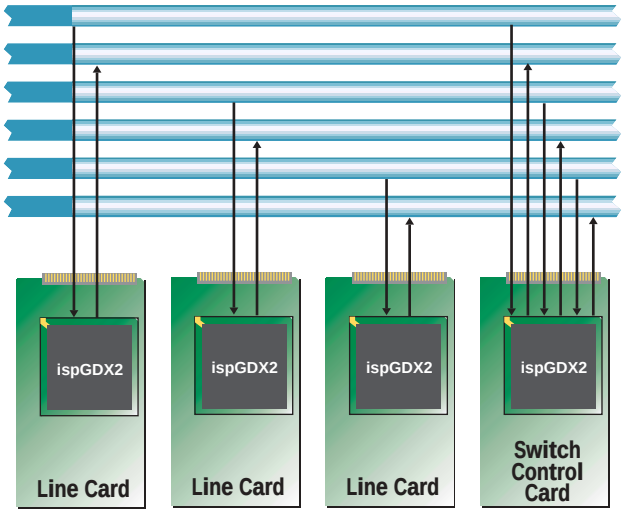
- Up to 38 Gbps bandwidth per ispGDX2 device
- In-system programmability and JTAG at board edge



Multi-Gigabit Serial Switched Backplane

The ispGDX2 offers a superior solution for signal routing and switching across backplanes. In the application below, the ispGDX2 devices provide the following features:

- One part type for implementing high-speed circuits on both line card and switch board
- Up to 13.6 Gbps bandwidth per ispGDX2
- Easy board side interface using sysIO and sysCLOCK features



ispGDX2 Family Attributes

Feature	ispGDX2-64*	ispGDX2-128*	ispGDX2-256*
I/Os	64	128	256
GDX Blocks	4	8	16
t_{PD}	3.0 ns	3.0 ns	3.5 ns
t_S	2.0 ns	2.0 ns	2.0 ns
t_{CO}	3.1 ns	3.1 ns	3.2 ns
f_{MAX}	330 MHz	330 MHz	300 MHz
Max. Bandwidth (SERDES)	3.5 Gbps	7.0 Gbps	13.6 Gbps
Max. Bandwidth (without SERDES)	11 Gbps	21 Gbps	38 Gbps
sysHSI Channels	4	8	16
Bus LVDS (Pairs)	32	64	128
PLLs	2	2	4
Package	100-Ball fpBGA	208-Ball fpBGA	484-Ball fpBGA

*Preliminary Information

ispGDX2 Advanced Packaging

Dimensions refer to package body size.

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ORCA ORT82G5 Evaluation Board

Evaluate 3.7Gbps SERDES + FPGA Quickly and Easily

Making the Right Choice...

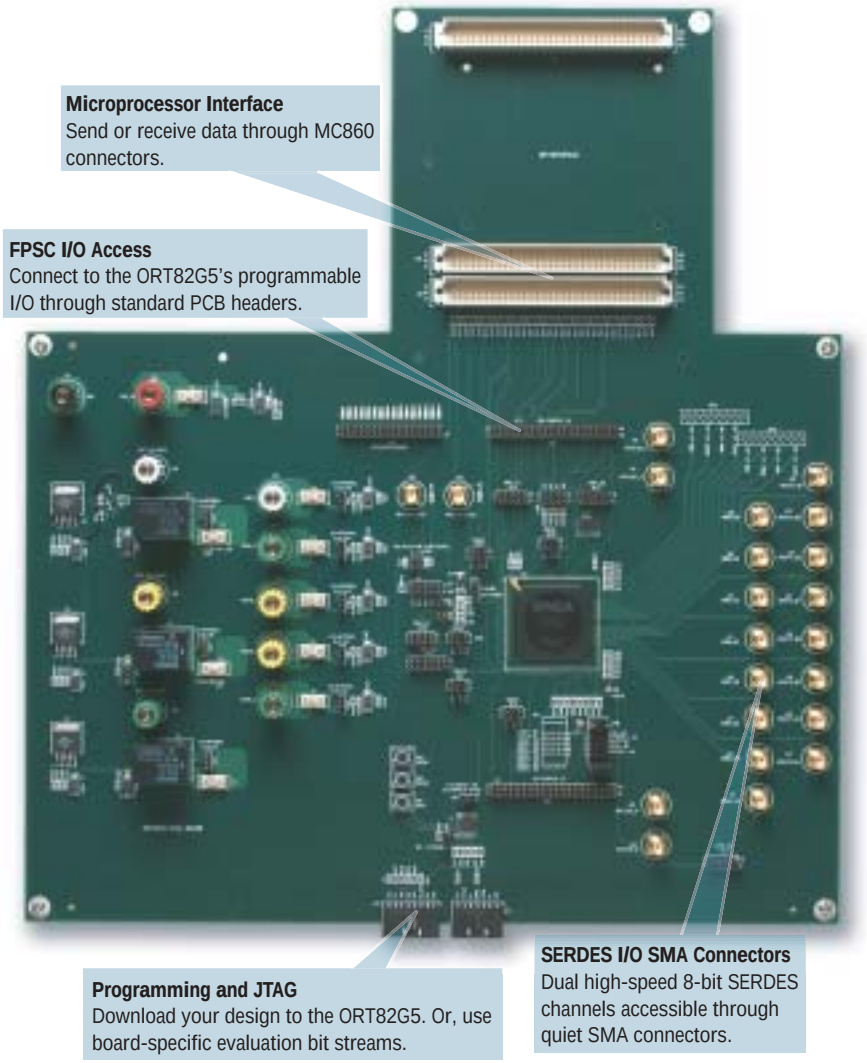
Choosing the right device to drive 3.7Gbits/s data over your backplane can be a critical decision, but evaluating your options shouldn't be complicated. Lattice has created the ORCA® ORT82G5 Evaluation Board so you can efficiently test the characteristics of a 3.7Gbits/s data stream generated by Lattice's ORT82G5 FPSC.

Examine Features Such as:

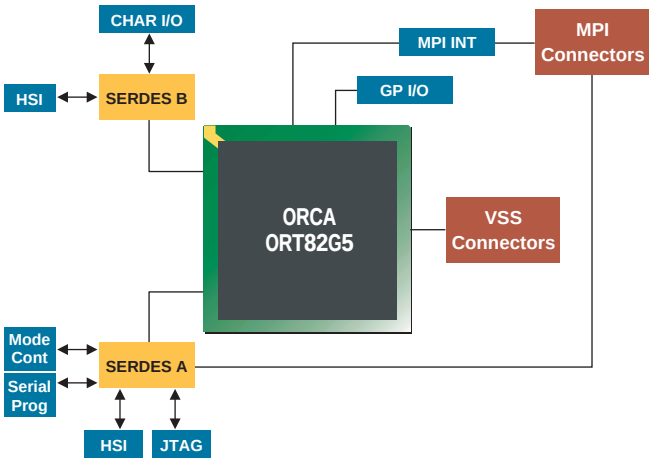
- Field Programmable System Chip (FPSC) flexibility and features
- ORT82G5 SERDES functionality and performance
- Programmable I/O capabilities
- Output strength and clarity
- Compliance to data transmission standards, from fiber channel to 10Gbit Ethernet (XAUI)

Working on an ORT82G5 Application?

Use the ORT82G5 Evaluation Board to help develop your application in an established and flexible environment. Download your design to the ORT82G5 for instant feedback.

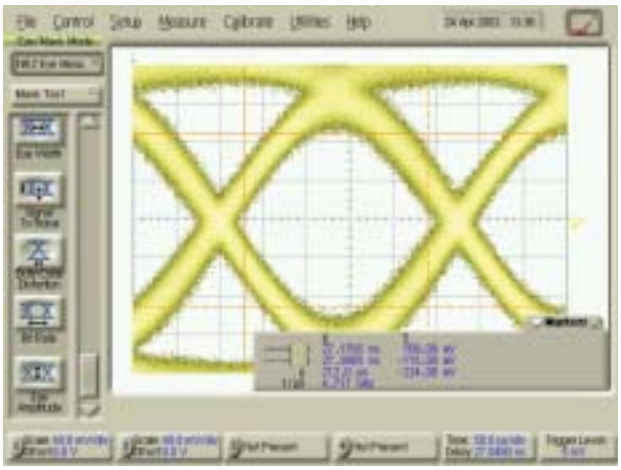


ORT82G5 Evaluation Board Block Diagram



Full Feature Set

- Push-button switches assert/de-assert the logic levels on the FPGA PRGMN, PRESET, and the SERDES reset.
- Interconnect test points for SERDES characterization.
- SMA connectors for differential inputs to the ORT82G5's four on-chip PLLs.
- Independent power supplies for the board and SERDES I/O.
- Downloadable programming bit streams are available from www.latticesemi.com for testing specific functions of the ORT82G5.



About the ORCA ORT82G5...

Lattice's ORT82G5 is a Field Programmable System Chip is based on the ORCA Series 4 architecture. The ORT82G5 integrates eight 3.7Gbits/s backplane transceiver channels and a full-duplex synchronous interface with built-in Clock and Data Recovery with a flexible FPGA logic core.

- Eight channels at 1.25 to 3.7 Gbits/s, exceeds XAUI specifications for 10Gbits/s Ethernet applications
- Optional 8b/10b encoding/decoding support on all channels
- Multi-channel alignment FIFOs available in 8b/10b mode
- More than 400K of usable FPGA gates, internal performance of >250MHz
- Four programmable PLLs
- Two extra embedded 4Kx36 dual-port RAM blocks
- Programmable I/O with programmable drive and slew rate control supports LVTTL, LVCMOS, GTL, GTL+, PECL, SSTL/3, HSTL, ZBT, DDR, LVDS, BLVDS and LVPECL
- 372 programmable user I/O

See www.latticesemi.com for complete specifications of the ORT82G5

ispLEVER™ Development Tools

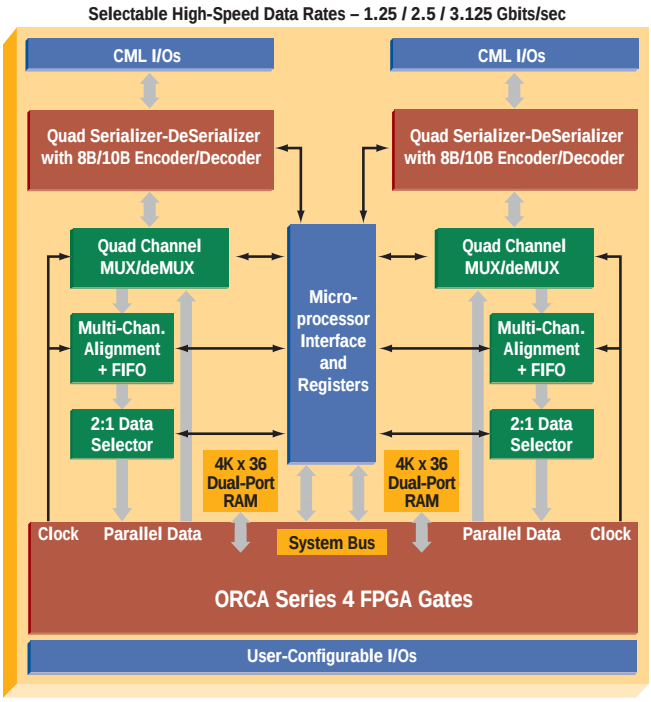
ispLEVER is an integrated software sysem for the development of all Lattice programmable logic devices, including the ORT82G5. The ispLEVER software incorporates ASIC design techniques and FPGA development methodologies that meet today's high-speed design demands.

Clear Your Eyes With the ORT82G5!

With data wavelengths now shorter than your backplane, clean and reliable signals are crucial. The ORT82G5 provides I/O capabilities that exceed today's tight standards. The ORT82G5 also features programmable pre-emphasis for transmission of reliable low-jitter SERDES signals, giving you more flexibility in applications utilizing Clock and Data Recovery (CDR).

With the ORT82G5 Evaluation board, you can measure the I/O performance of the ORT82G5 in an environment you control. The signal to the left is the actual data-eye of a 3.7Gbps SERDES transmission across 26 inches of FR-4 backplane, generated by the ORT82G5 using 25% pre-emphasis.

ORCA ORT82G5 Block Diagram



- Included with the ORT82G5 Evaluation Board:
  - ORT82G5-2BM680 device
  - ORCA download cable
  - Board schematic and bill of materials
- Available on www.latticesemi.com:
  - ORT82G5 Eval Board User Manual and Tutorial
  - IBIS and HSPICE models, and BSDL files
  - Schematic and Gerber files
  - Evaluation bit streams

Applications Support
1-800-LATTICE (528-8423)
(408) 826-6002
techsupport@latticesemi.com

Lattice Semiconductor Corporation
www.latticesemi.com

ORCA ORT8850 Evaluation Board

8 x 850Mbits/s SERDES Plus up to 899K FPGA Gates on One Chip!

Making the Right Choice

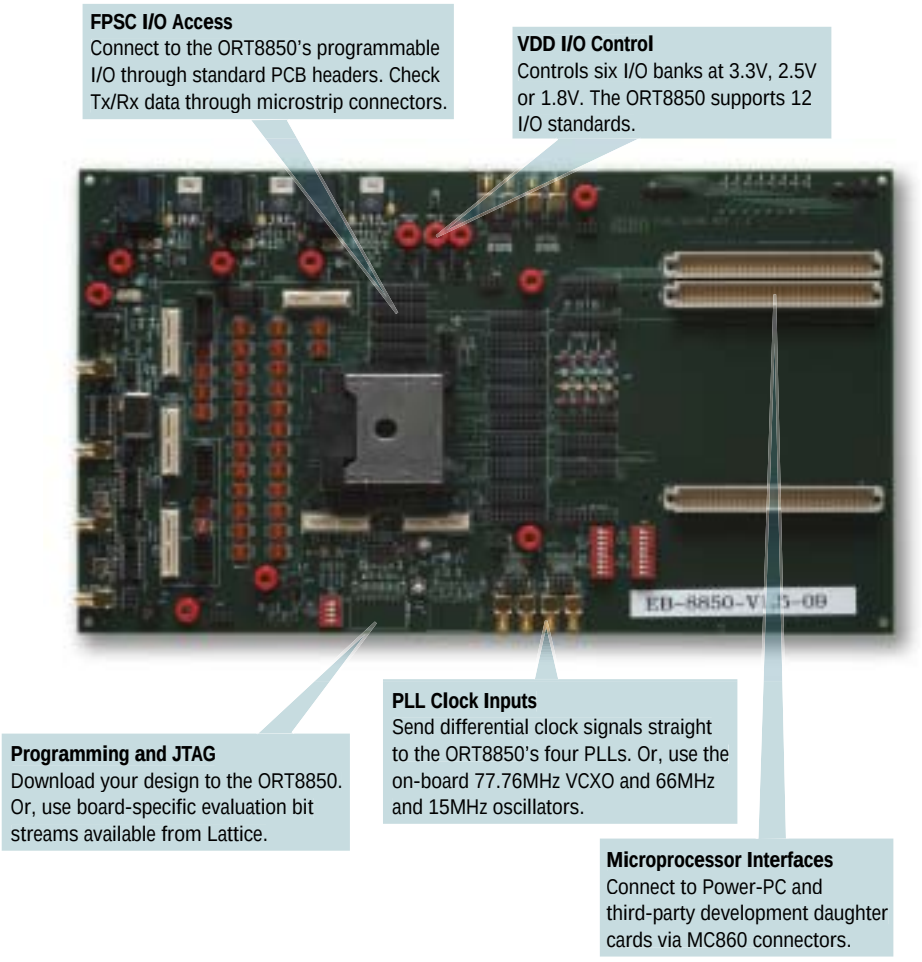
Choosing the right backplane transceiver solution is an important investment decision, but evaluating your options shouldn't be complicated. Lattice has created the ORCA® ORT8850 Evaluation Board so you can efficiently test the performance of a completed PCB design based on the ORT8850 Field Programmable System Chip (FPSC) architecture.

Examine Features Such as:

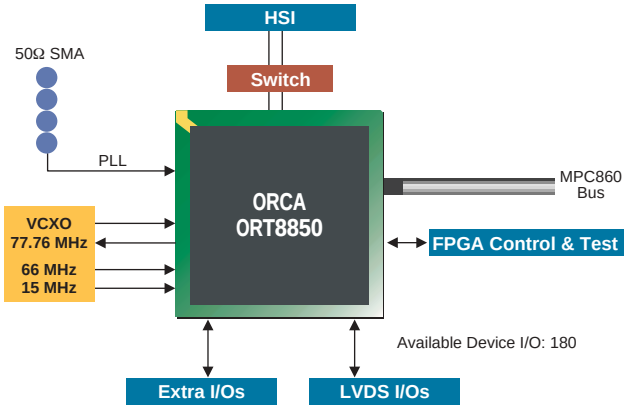
- FPSC flexibility
- ORT8850 performance and features
- Programmable I/O capabilities
- Output strength and clarity

Working on an ORT8850 Application?

Use the ORT8850 Evaluation Board to help develop your customized ORT8850 solution in an established and flexible environment. Download your design to the ORT8850 for instant feedback.

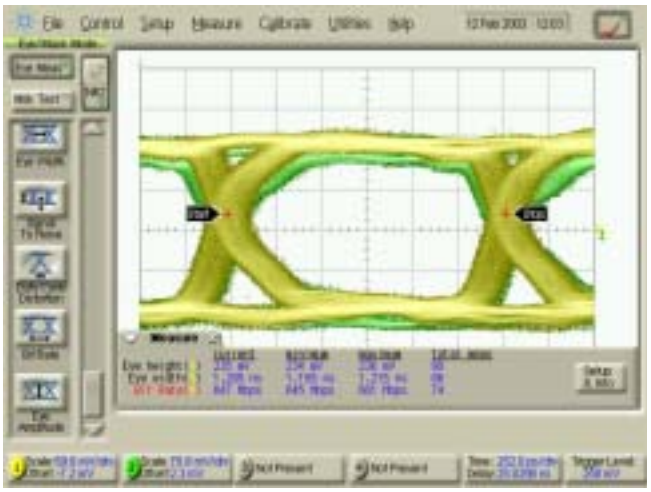


ORT8850 Evaluation Board Block Diagram



Full Feature Set

- 180 of the ORT8850H's I/Os are accessible on the board. These include 32 HSI (LVDS) I/Os and other I/Os directly from up to 899K FPGA system gates.
- Includes a regulated power supply for easy set-up.
- Downloadable programming bit streams are available from www.latticesemi.com for testing specific functions of the ORT8850.



About the ORCA ORT8850...

Lattice's ORT8850 is a Field Programmable System Chip based on the ORCA Series 4 Architecture. The ORT8850 integrates eight 850Mbits/s backplane transceiver channels with a flexible FPGA logic core. Features of the ORT8850 include:

- Up to 899K of usable FPGA system gates and 147Kb Embedded RAM (ORT8850H)
- Internal performance of >250MHz
- LVDS I/Os compliant with EIA-644
- Multi-channel alignment FIFOs available
- SONET scrambler/descrambler
- Four programmable PLLs
- 297 programmable user I/O (ORT8850H)

See www.latticesemi.com for complete specifications of the ORT8850

ispLEVER™ Development Tools

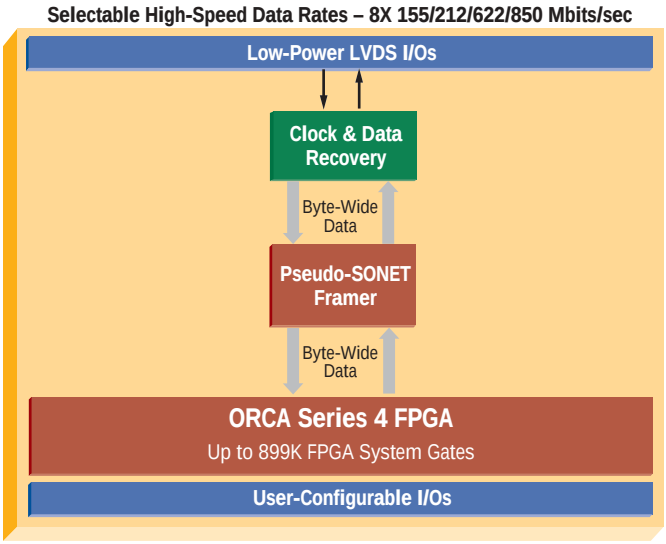
ispLEVER is an integrated software sysem for the development of all Lattice programmable logic devices, including the ORT8850. The ispLEVER software incorporates ASIC design techniques and FPGA development methodologies that meet today's high-speed design demands.

Sharpen Your Focus With the Eye of the ORT8850

Clean data transmission has always been important, but with data wavelengths getting shorter than your backplane, it's crucial! We've focused our engineering efforts on the ORT8850 I/O structure to provide high-quality data transmission exceeding today's tight standards.

With the ORT8850 Evaluation board, you can measure the I/O performance of the ORT8850 in an environment you control. The signal to the left is an actual data-eye of a PRBS pattern generated by the ORT8850's LVDS I/Os at 880Mbits/sec.

ORCA ORT8850 Block Diagram



- Included with the ORT8850 Evaluation Board:
  - ORT8850H-BM680 device
  - ORCA Download Cable
  - Power supply
  - Board schematic and bill of materials
- Available on www.latticesemi.com:
  - ORT8850 Eval Board User Manual and Tutorial
  - IBIS and HSPICE Models, and BSDL files
  - Schematic and Gerber files
  - Evaluation bit streams

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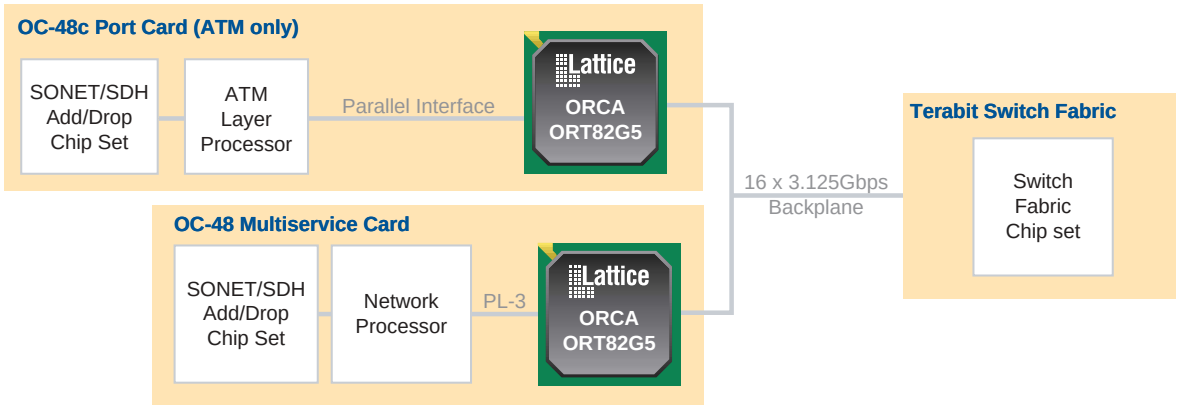
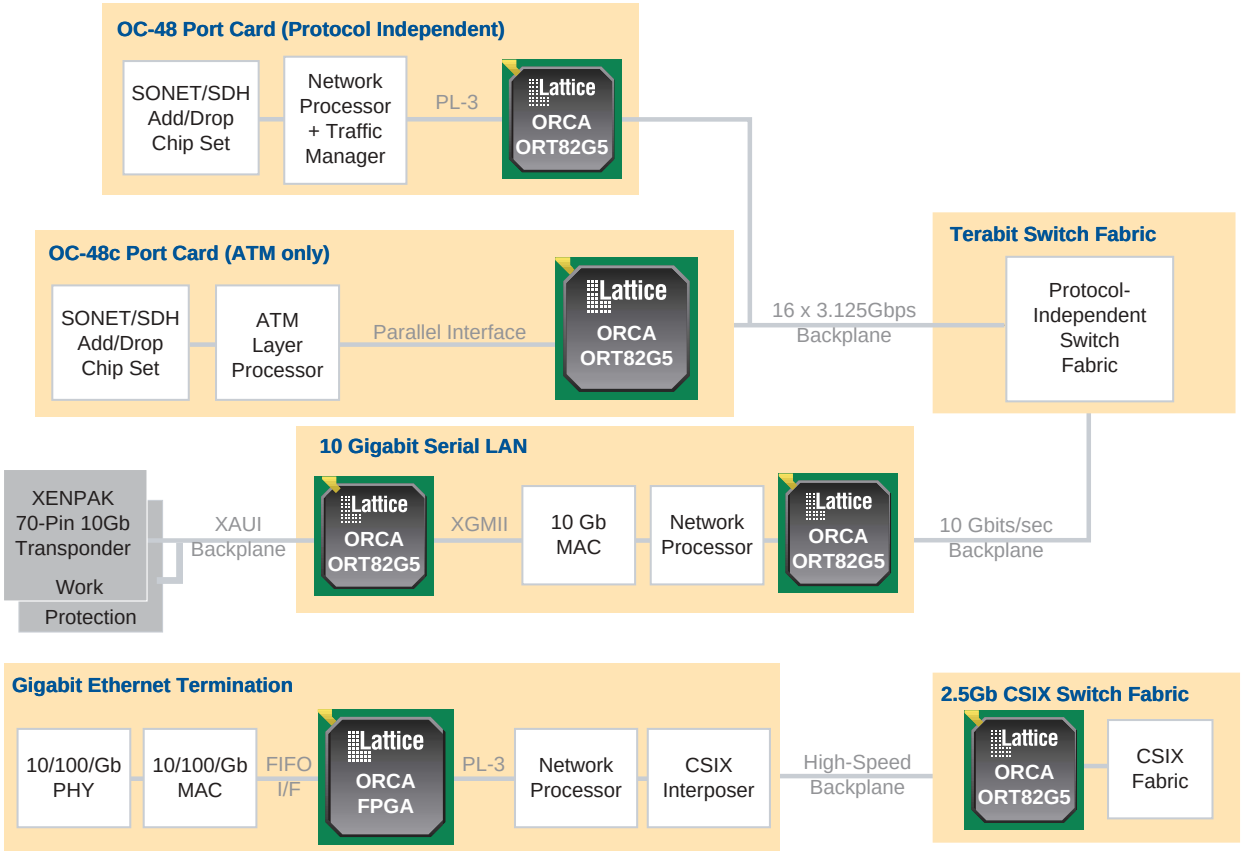
ORCA ORT82G5 Applications

The World's Fastest Programmable SERDES Solution!

ORT82G5 in Metro Access Applications



ORT82G5 in Multi-Service Switching and Routing



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Lattice Semiconductor Corporation
www.latticesemi.com
September 2002

10 Gigabit Ethernet XGXS Intellectual Property Core

April 2003 **Product Brief**

Overview

The 10 Gigabit ethernet eXtender Sublayer (XGXS) Intellectual Property (IP) Core enables creation of system solutions for 10 Gigabit Ethernet applications as defined by IEEE 802.3ae. This IP Core targets the programmable array section of the ORCA® ORT82G5 FPSC and provides a bridging function between 10 GbE Media Independent Interface (XGMII) and 10 GbE Attachment Unit Interface (XAUI) devices. It is implemented as a soft IP core for flexibility.

The XGMII interface block provides an interface to 10 Gbits/s Ethernet MACs. XGMII is a 156 MHz double data rate, parallel short-reach (typically less than 2 inches) interconnect interface.

XAUI is a high-speed interconnect that offers reduced pin count and has the ability to drive up to 20 inches of PCB trace on standard FR-4 material. Each XAUI interface is comprised of 4 self-timed 8b10b encoded serial lanes, each operating at 3.125 Gbits/s.

The IP core from Lattice Semiconductor is provided with all implementation scripts, test benches, and documentation to allow customers to integrate the functions for 10GbE LAN/WAN applications and also for modification of the core to meet differing application needs.

10 Gigabit Ethernet ORT82G5 and IP Core Features

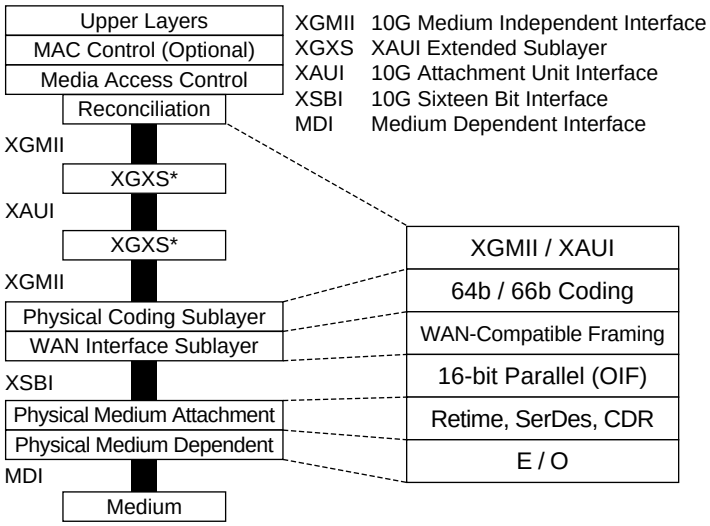
The embedded portion of the ORT82G5 includes:

- Eight channels of 3.125 Gbps serializer/deserializer with 8b10b encoding/decoding
- Fibre-channel and XAUI compliant lane-by-lane synchronization
- Lane deskew function
- PRBS generator/checker for selftest
- Microprocessor interface programmable via the ORCA Series 4 system bus

The soft XGXS IP core implements the interface functions needed to take data from XAUI lanes to an XGMII interface device (e.g. MAC) and vice-versa. The programmable logic implementation allows for changes to the core to reflect changes in the standards definition in the future.

The XGMII consists of 4 lanes, labeled [0:3], and 1 clock in both the transmit and receive directions. Each lane is an 8-bit data path plus a control signal. Double Data Rate (DDR) signaling is used to transfer 312.5 MBytes/s per lane with a 156.25 MHz clock. The data and control lines are sampled on both the rising and falling edges of the clock. XGXS's location in the 10GbE protocol stack is shown in Figure 1 on the following page

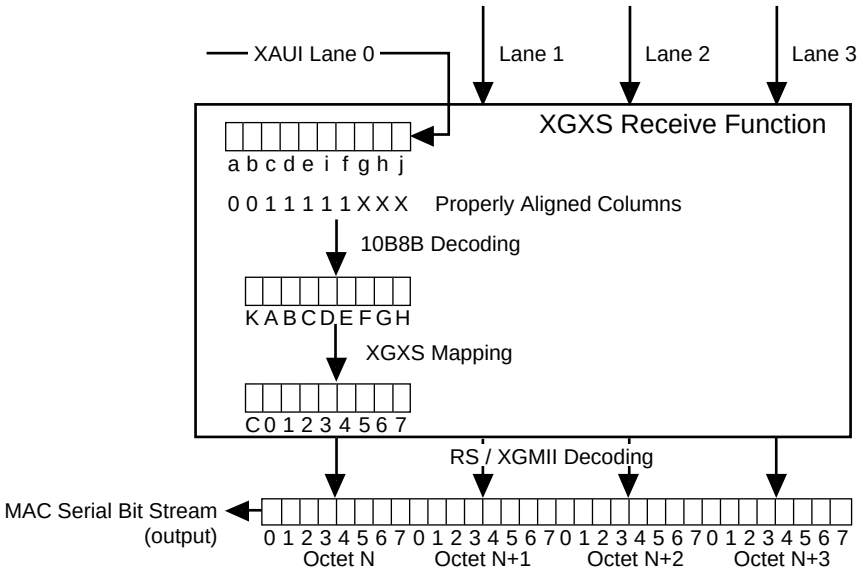
Figure 1. XGXS Location in Protocol Stack



Notes:
1. Adding the WIS makes the WAN PHY
2. * Denotes Optional Sublayer

The receive path, shown in Figure 2, is the data path from the XAUI to the XGMII interface. It maps 8b10b decoded XAUI data to XGMII data and optionally transmits the data off-chip via the 36-bit 156Mhz DDR XGMII interface.

Figure 2. XGXS Receive Path Dataflow



The transmit path, shown in Figure 3, is the data path from XGMII to XAUI. The XGXS transmit path maps the 36-bit DDR XGMII data and control to the 8b10b transmission code. The XGMII data and control are clocked by DDR registers in the I/O blocks. A slip buffer performs clock compensation between the external clock and the internal synthesized 156.25 Mhz clock. Data and control read from the buffer are then passed into the idle generation logic.

Figure 3. XGXS Transmit Path Dataflow

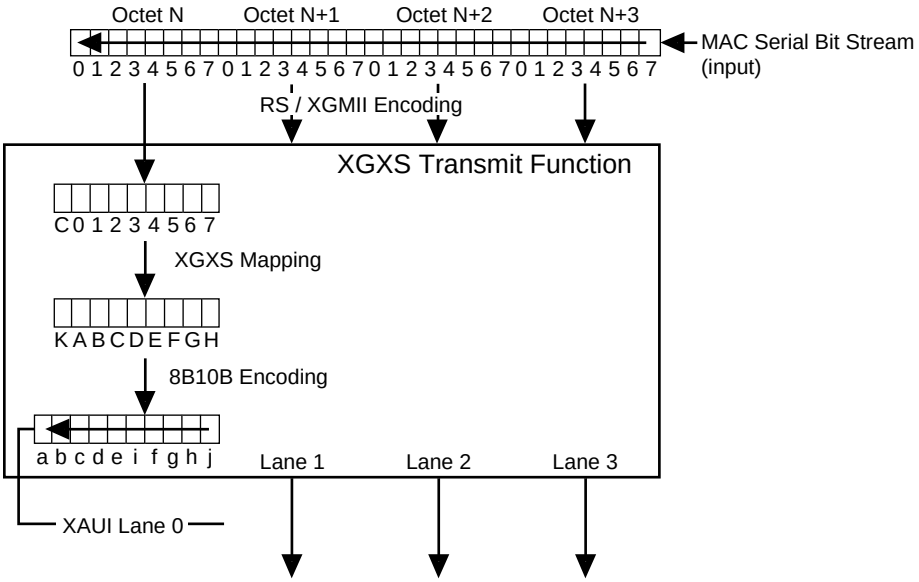


Figure 4. Generator/Checker Interface

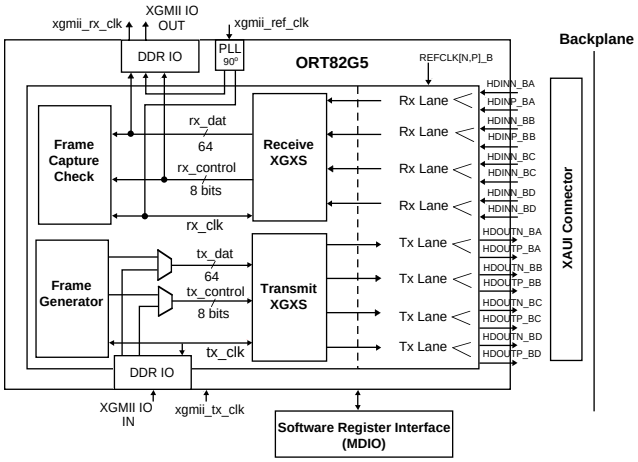
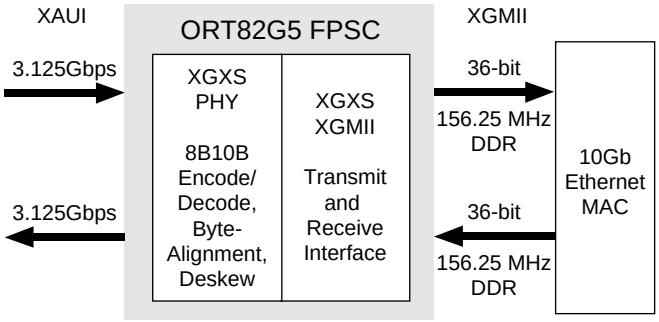


Figure 5. Interface with External MAC

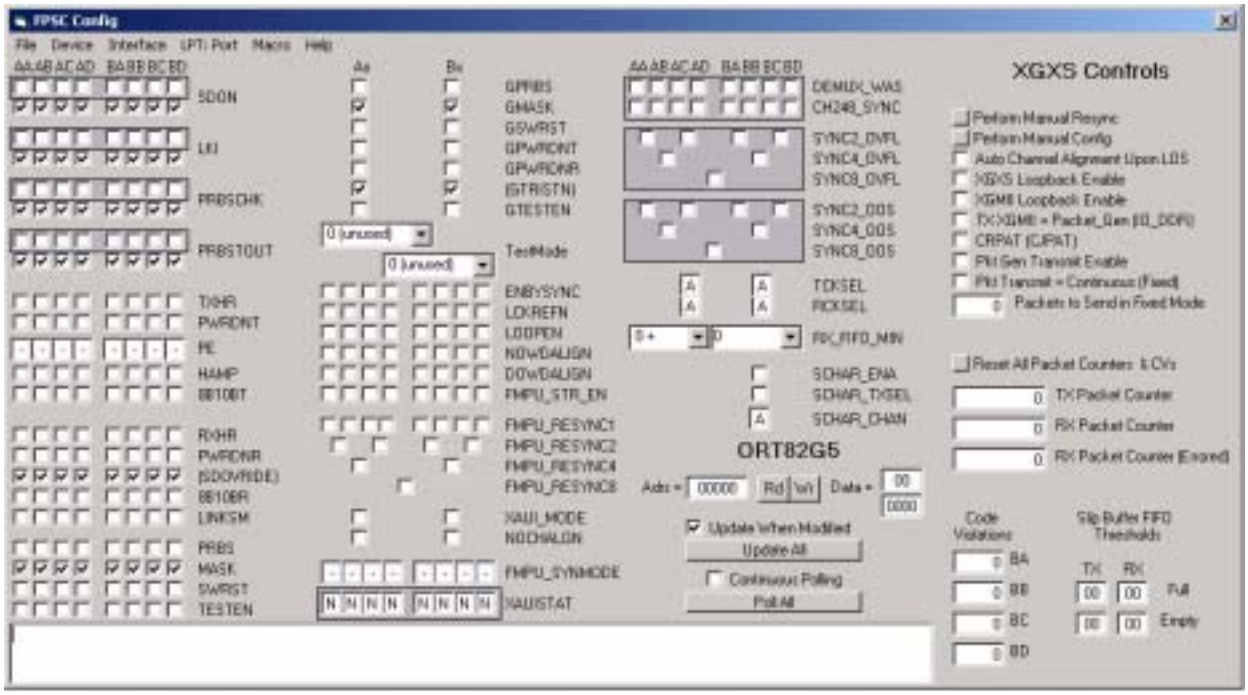


For Ethernet, the idle generation state machine generates the random /A/, /K/ and /R/ characters. The Idle signal /I/ at the XGMII end is mapped to a random sequence of /A/, /R/ and /K/ code groups to reduce radiated emissions and help designers meet EMI requirements. The /A/ code-groups are included for the purpose of lane alignment and, to that end, have a guaranteed minimum spacing of 16 code-groups. The /K/ code-groups contain a comma sequence and are used by the XAUI receive section to establish code-group alignment. The /R/ code-groups are used for clock-compensation and may be inserted or deleted by the XGXS to accommodate for differences between transmit and receive clocks.

The ORT82G5 XGXS interfaces to XGMII in one of two ways:

- A built-in 64-bit 156Mhz XGMII CRPAT/CJPAT packet generator/checker (Figure 4).
- A standard 36-bit IO DDR interface (e.g. to a MAC) (Figure 5).

Figure 6. ORCAstra GUI Interface



Using the ORCAstra® control center, a graphical user interface similar to the one shown in Figure 6 performs real time modifications and monitoring. In addition to the FPSC specific functions shown in Figure 6, the GUI has entries for XGXS specific registers, such as FIFO threshold, loopback modes control, and push buttons to run specific synchronization algorithms. Control over the internal packet generator functions, and monitoring of the internal packet generator error outputs are also available.

Other Information

Product briefs, data sheets, application notes and other information on many of the products used in the above system solutions are available from Lattice Semiconductor. FPSC solutions are also highlighted on the Lattice Semiconductor website at: http://www.latticesemi.com.

Ordering Information

Implementing a design in an ORT82G5 requires the ispLEVER™ software and an ORT82G5 FPSC Design Kit. For ordering information, please contact your local Lattice Semiconductor sales representative or visit the Lattice Semiconductor website.

ORT42G5 and ORT82G5 High-Speed Backplane Measurements

April 2003 Technical Note TN1027

Introduction

The Lattice ORT82G5 FPSC device contains two Quad-SERDES blocks. The Lattice ORT42G5 FPSC device contains one Quad-SERDES block. Each SERDES (SERializer/DESerializer) provides a serial high-speed backplane transceiver interface, operational at data rates up to 3.7 Gbit/s.

This document illustrates SERDES high-speed backplane capabilities, through a series of laboratory tests. The Tyco HM-Zd Backplane Evaluation system[1] was used extensively in these tests. Three different configuration experiments are described:

- Eye-Diagram Experiment I – Shows performance over a standard reference backplane.
- Eye-Diagram Experiment II — Shows performance variations with signal pre-emphasis, board layers and trace length.
- Data-Rate Experiment — Shows data rate limits measured for 26 and 40 inch FR4 path lengths.

Bit-error rate and eye-diagram measurements are used to evaluate link performance and margins. Error-free performance is observed through various backplane connections and over different operating conditions, for test intervals of several minutes. The effects and benefits of transmitter pre-emphasis and amplitude adjustment are illustrated. Finally, some general application recommendations are made for high-speed backplane interconnection design.

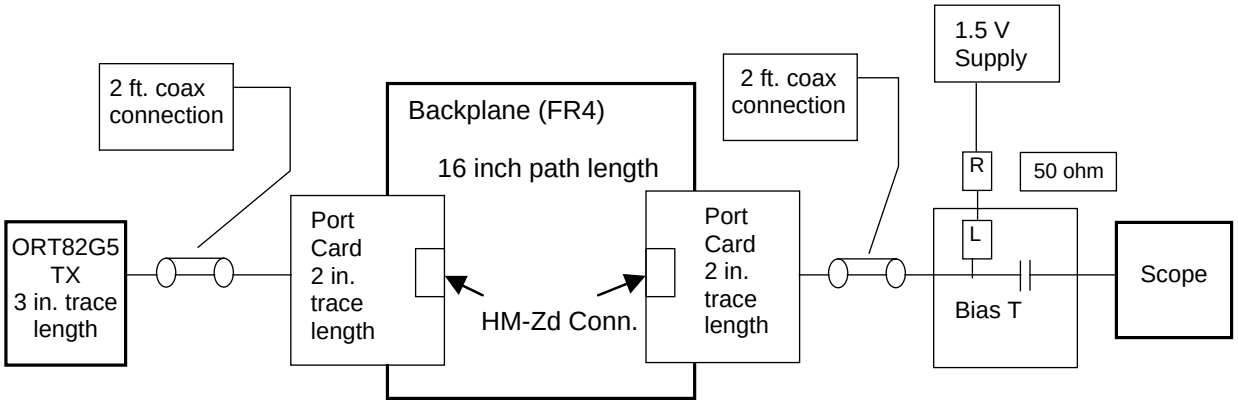
Eye-Diagram Experiment I

Eye-diagram signal waveforms observed at the receive end of PCB interconnection paths were recorded. This measurement displays the effect of various system error contributions on received signal integrity. A series of such measurements made while driving through the Tyco test backplane[1] are described in this section.

Test Equipment

– ORT82G5 evaluation board
– Tyco Electronics XAUI backplane with two port cards[1]
– HPE3648A power supplies
– HP8133A clock source
– Temptronic E3648A thermal soaker
– PicoSecond 5575A Bias-T
– Agilent 86100A DCA oscilloscope

Figure 1. Eye-Diagram Test Setup



Test Setup

Figure 1 shows the test setup used to measure the data eye-openings discussed in this document. The TX signal comes directly from an ORT82G5 high-speed serial output. A pseudo-random signal pattern generated in the ORT82G5 was processed through an internal 8B/10B encoder.

Test Setup Parameters

– ORT82G5 680 PBGAM plastic ball grid array (wire-bond), -3 speed grade
– Power Supply = 1.5 V
– Ambient Temperature = 25° C
– Data Pattern = PRBS 2^32 - 1 with 8B/10B encoding

PCB Specification

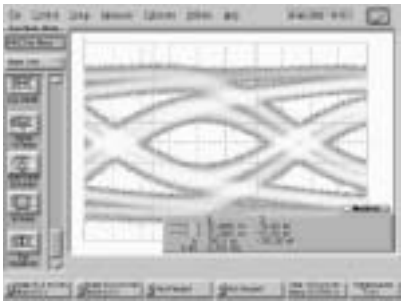
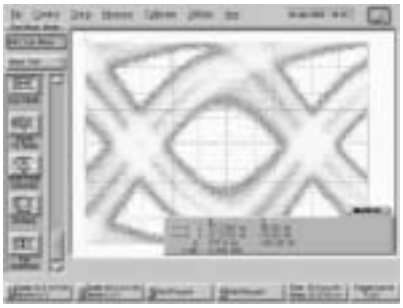
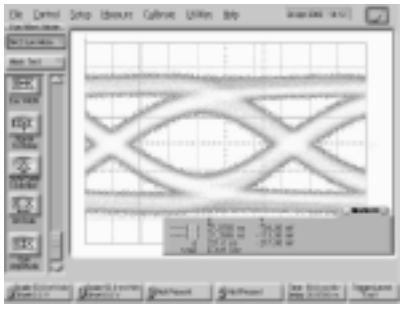
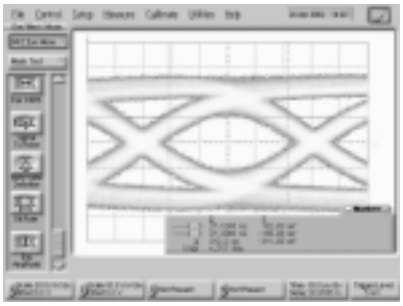
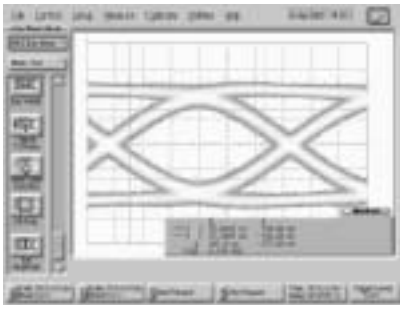
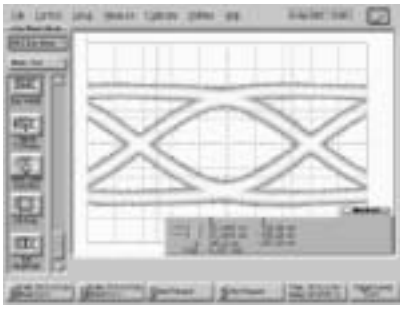
– The 2-inch PWB section (port card) is composed of 6 mil wide (1/2 oz. copper thickness) 100 Ohm differential impedance traces
– Backplane - 200 mils thick, 14 layers, Nelco 4000-6 FR4
– All signal layers are 10 mil wide (1/2 oz. copper thickness) traces designed for 100 Ohm differential impedance
– All signal layers buried and surrounded by GND planes
– Port Card - 93 mils thick, 14 layers, Nelco 4000-4 FR4
– Total trace length: 3 + 2 + 2 + 16 = 23 inches

Typical Eye-diagram Measurements

A typical application might have a total PWB trace path length of 12 to 24 inches, between two interconnected devices. This section shows a series of eye-diagram measurements for a 23 inch path length. Receiver eye-diagram measurements can provide an excellent indication of expected link performance. Data rate and pre-emphasis levels were varied. Eye-opening time and amplitude are indicated below each waveform. All tests in this section were performed at room temperature and nominal supply voltage.

The ORT42G5 and ORT82G5 high-speed outputs provide software programmed pre-emphasis parameters of 0%, 12.5% or 25%. Pre-emphasis compensates for the high frequency losses that a typical physical interconnection system exhibits. Enabling pre-emphasis provides increased interconnection path length capability and/or increased eye-opening for a given path length. In general, pre-emphasis should only be enabled where needed, since there is a slight increase in power dissipation and EMC radiation associated with this feature.

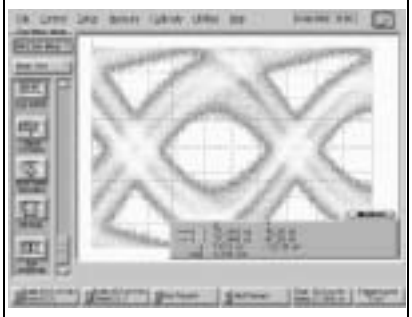
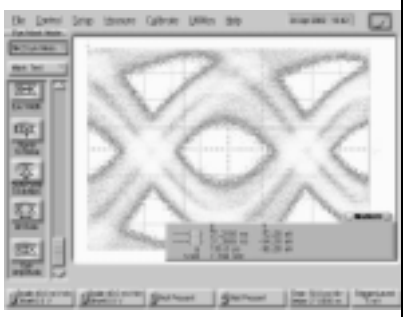
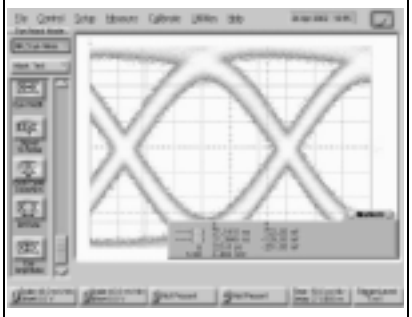
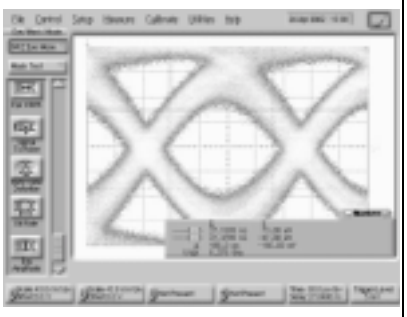
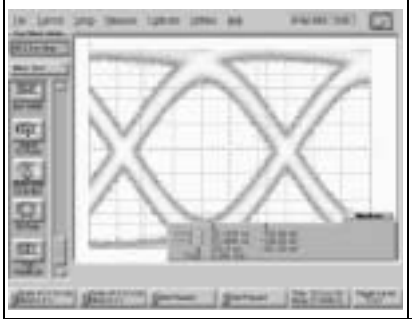
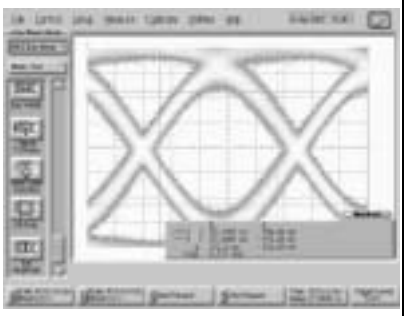
Figure 2. Receiver Eye Patterns at 3.125 and 3.3 Gb/s Over a 23 inch Path Length

	3.125Gb/s	3.300Gb/s
00.0% Pre-emphasis		
	186 ps 155 mV	177 ps 145 mV (50mV/div)
12.5% Pre-emphasis		
	221 ps 217 mV	212 ps 211 mV
25.0% Pre-emphasis		
	241 ps 277 mV	240 ps 267 mV

In Figure 2, note that the vertical scale is 100mV/div, except in the top-right eye pattern where it is 50mV/div.

The eye-opening amplitudes in the above Figure can be compared to the 80 mV eye requirement specified in the ORT42G5 and ORT82G5 data sheet. At all data rates, the eye amplitude without pre-emphasis is above the required level.

Figure 3. Receiver Eye Patterns at 3.5 Gb/s and 3.7 Gb/s Over a 23 inch Path Length

	3.500Gb/s	3.700Gb/s
00.0% Pre-emphasis		
	153 ps 122 mV	139 ps 96 mV
12.5% Pre-emphasis		
	197 ps 238 mV	186 ps 160 mV
25.0% Pre-emphasis		
	223 ps 251 mV	212 ps 224 mV

The eye-openings are smaller in the above Figure because of the higher data rates, where the path losses are greater. At these data rates 25% pre-emphasis must be used to achieve a comfortable margin above the 80 mV required eye-opening level.

In Figure 3, note that the vertical scale is 50mV/div in each eye pattern.

Eye-Diagram Experiment II

This section describes some additional, detailed measurements made with a preliminary version of the Tyco XAUI backplane reference system. Note that it has some differences in the PCB description, as compared to section 2. This particular backplane had multiple traces of equal length, run on different PCB layers.

Test Equipment

– ORT82G5 evaluation board.
– Tyco XAUI Backplane with fixed lengths of 4, 16 & 24in.
– HPE3630A, HPE3610A, HP6213A power supplies
– HP8656B clock source
– Temptronic Thermostream TP04100A-1
– PicoSecond 5575A Bias-T
– Agilent 86100A DCA oscilloscope

Test Setups

Figure 4 shows the test setup used to measure the data eye-openings discussed in this section.

Figure 4. Eye-Diagram Test Setup

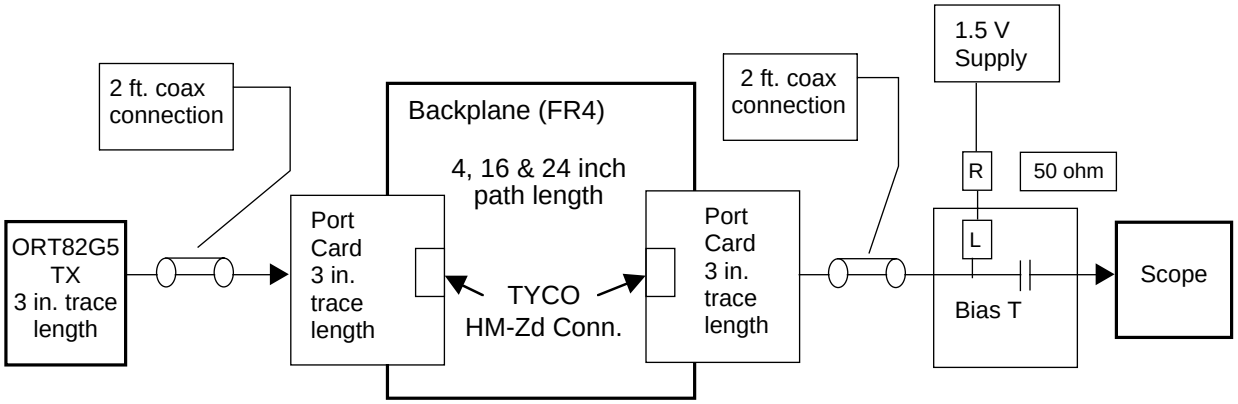
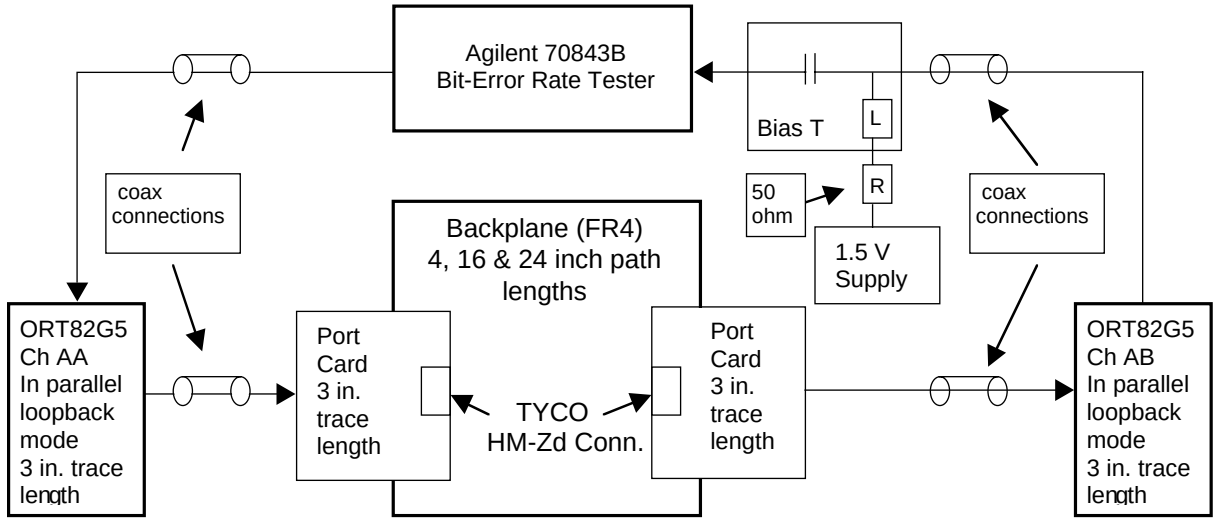


Figure 5 shows the test setup used for bit-error rate measurements discussed in this section.

Figure 5. Bit Error Rate Test Setup



Test Setup Parameters

– ORT82G5 680 PBGAM plastic ball grid array (wire-bond), -3 speed grade
– Power Supply = 1.5 V
– Ambient Temperature = 25 degree C
– Data Pattern = PRBS 2^7 - 1

Backplane Specification

– The 3 inch PWB section (port card) is composed of 10 mil wide 100 Ohm differential impedance traces
– Backplane - 205 mils thick, 14 layers, Nelco 4000-6 FR4
– All signal layers designed for 100 Ohm differential impedance
– All signal layers buried and surrounded by GND planes
– Line Card - 115 mils thick, 10 layers, Nelco 4000-4 FR4
– The backplane and line card details can be obtained from Tyco Electronics

The HM-Zd Evaluation System consists of 16 unique testable differential pairs for each interconnection length, as listed in Table 1. The basic information for each signal pair is given below. From our measurements, layer 4 and layer 1 were determined to be the best and worst from a signal integrity standpoint. Since the signal layer geometry is the same for both layers, the difference in signal integrity between the two layers is probably due to the difference in the via stub seen at layer 1 versus layer 4.

Table 1. PWB Trace Signal Pair Descriptions

Signal Pair Number	Line Card Trace Width	Backplane Trace Width	Signal Layer Connection
1	8 mils	12 mils	1
2,5,7	8 mils	12 mils	4
3,6,8	8 mils	12 mils	2
4	8 mils	12 mils	3
9	5 mils	12 mils	1
10	5 mils	12 mils	4
11	5 mils	12 mils	2
12	5 mils	12 mils	3
13	5 mils	8 mils	1
14	5 mils	8 mils	4
15	5 mils	8 mils	2
16	5 mils	8 mils	3

Figure 6 is a plot showing the variation in data eye-opening between the various 33" signal pairs (24" backplane + 6" line card + 3" ORT82G5 board). For the 0% pre-emphasis case the variation between the best signal pair (#4) and the worst signal pair (#13) is 214mV - 157mV = 57mV (26%). The specified minimum data eye-opening at the receiver for the ORT42G5 and ORT82G5 SERDES macro is 80mVp-p differential. Therefore, all signal pairs have adequate system performance without pre-emphasis.

Figure 6. 33 Inch Path Length Eye-Openings

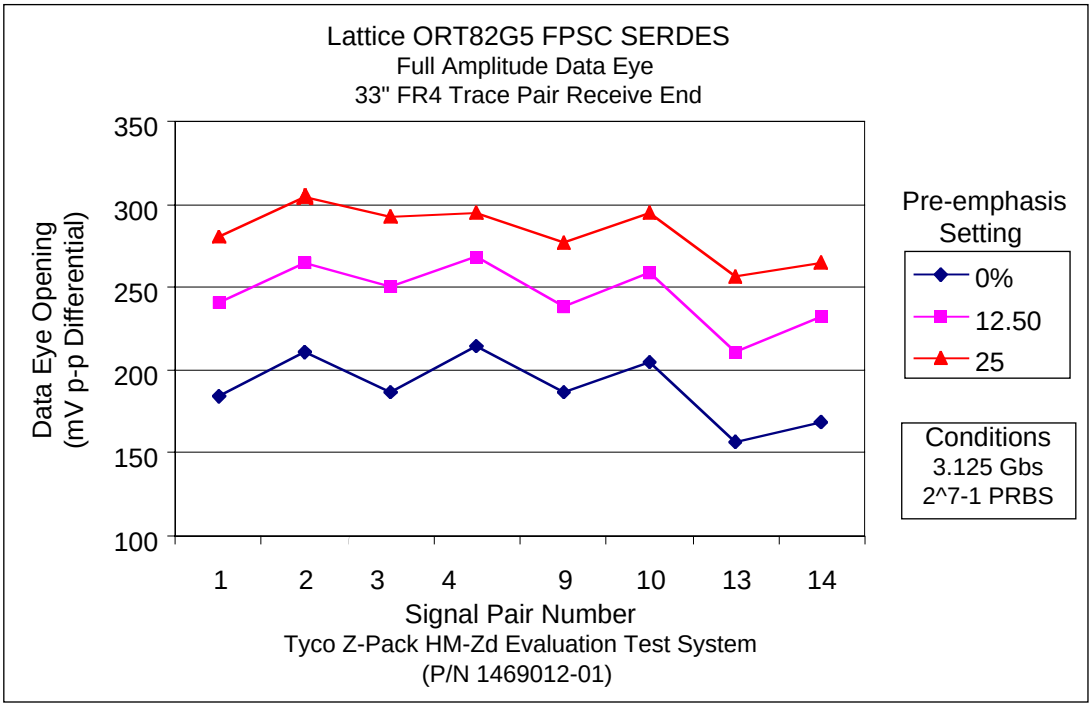


Figure 7 and Figure 8 are plots showing the variation in data eye-opening for signal trace pair #2 between the three trace lengths (24", 16" and 4" backplane + 6" line card + 3" ORT82G5 board). Notice that for the 4" and 16" backplane traces 25% pre-emphasis actually degrades the data eye. Figure 7 shows data eye-openings for full amplitude transmit buffer signal outputs. Figure 8 shows data eye-openings for one half amplitude transmit buffer signal outputs. The one half amplitude mode is used as a power saving feature and is set through a microprocessor register bit. Also shown in Figures 7 and 8 are the power consumption values for the Transmit Output buffer power supply (VDDOB).

Figure 7. Pair 2 Full-Amplitude Eye-Opening vs. Pre-Emphasis and Trace Length

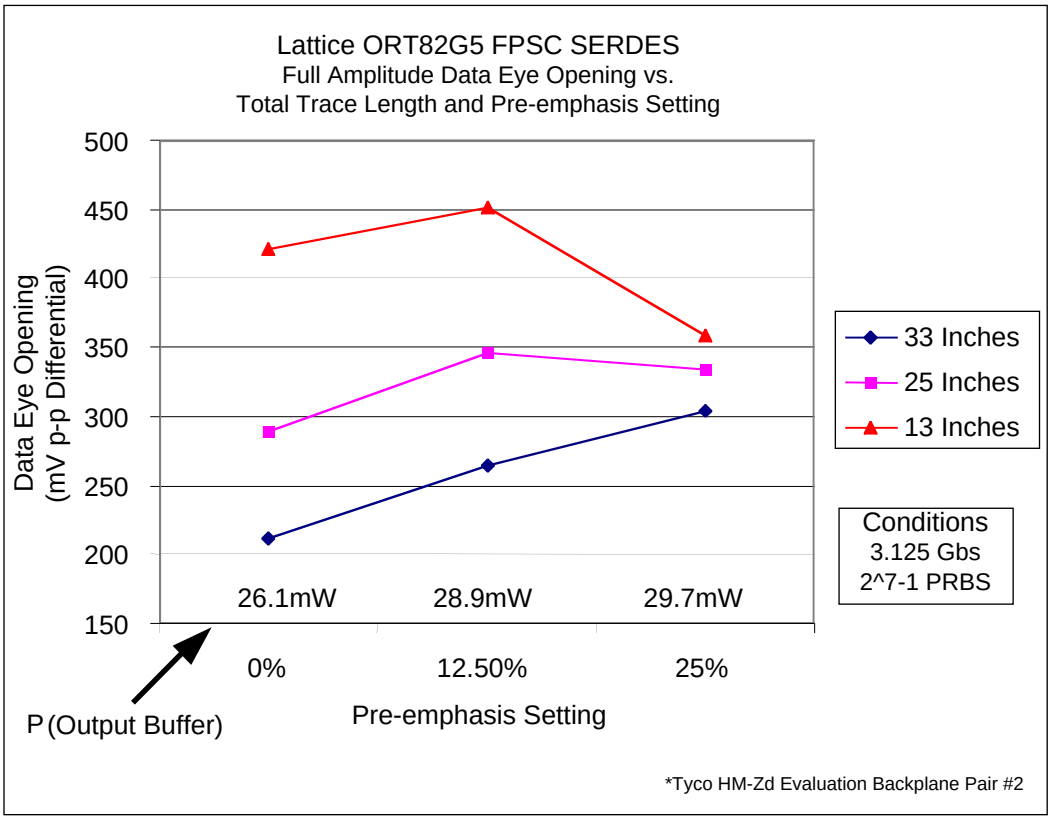
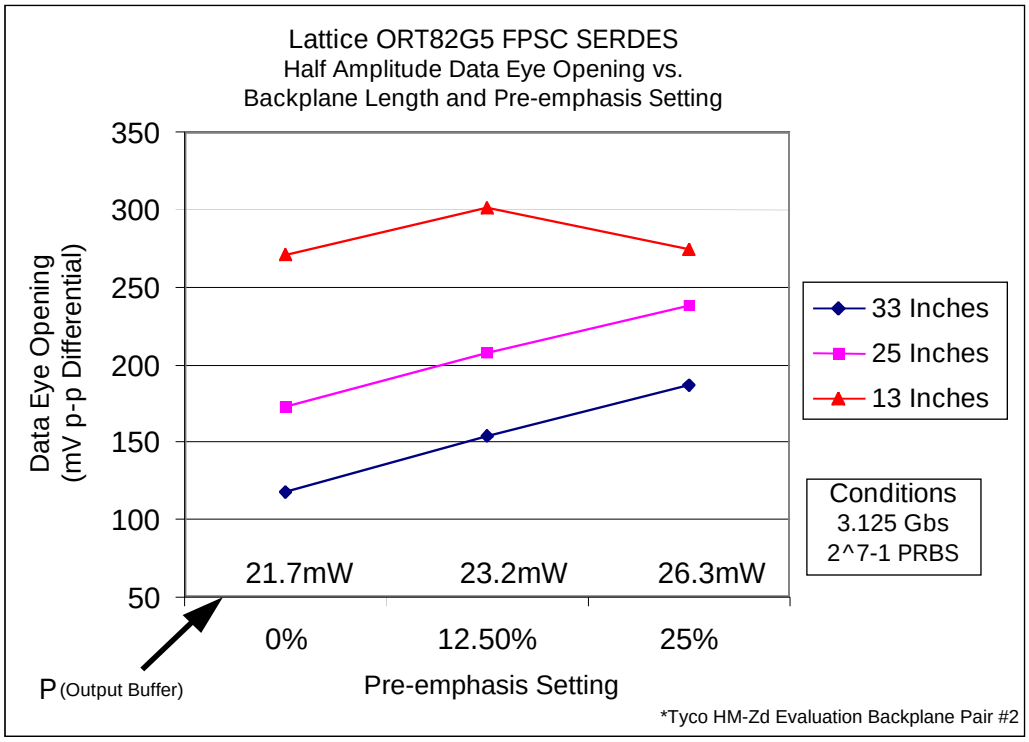


Figure 8. Pair 2 Half-Amplitude Eye-Opening vs. Pre-Emphasis and Trace Length



The nominal TX output buffer power consumption vs. pre-emphasis and output amplitude settings is shown in the following table (data taken from Figures 5 and 6).

Table 2. Nominal TX Output Power vs. Parameter Settings

Pre-Emphasis	0%	12.5%	25%
Half-Amplitude	21.7 mW	23.2 mW	26.3 mW
Full-Amplitude	26.1 mW	28.9 mW	29.7 mW

The power penalty/benefit of these settings can be determined by comparing values in the table.

Figure 9 and Figure 10 are plots showing the variation in vertical data eye-opening for signal trace pair #13. Notice the difference in data eye-opening between the measurements for signal trace pair #2 and signal trace pair #13. The primary difference between these two trace pairs is trace width and layout geometry (see Table 1).

Figure 9. Pair 13 Full-Amplitude Eye-Opening vs. Pre-Emphasis and Trace Length

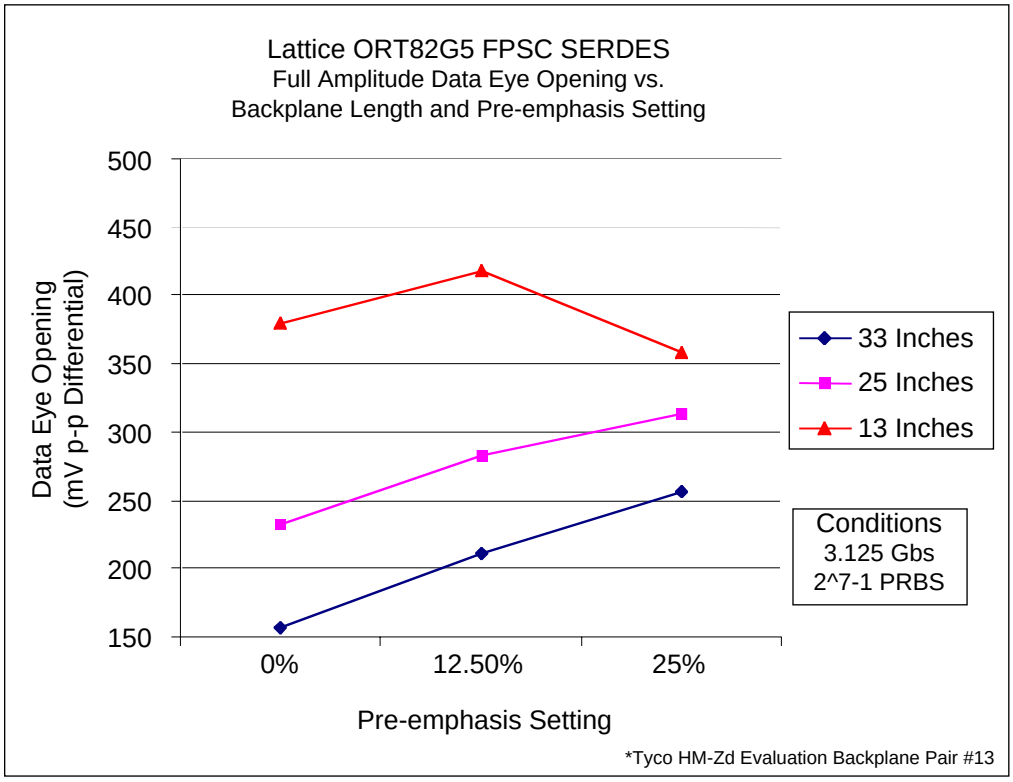


Figure 10. Pair 13 Half-Amplitude Eye-Opening vs. Pre-Emphasis and Trace Length

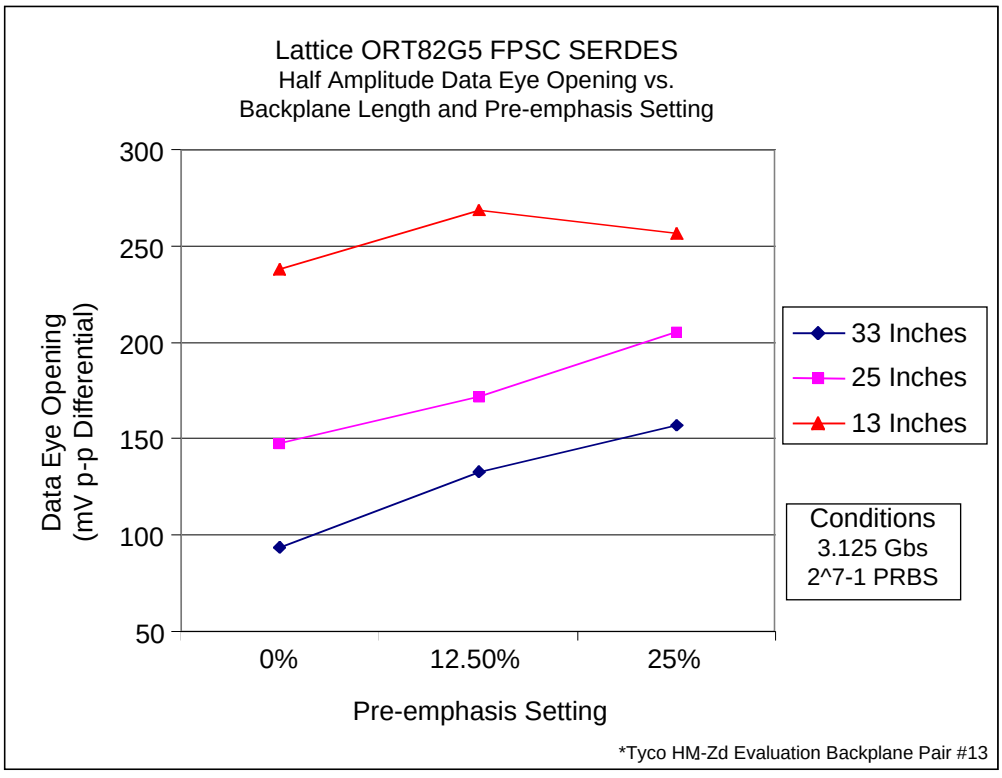


Figure 11 shows the horizontal eye-opening as a function of trace length and pre-emphasis for signal trace pair #2 at full transmit amplitude. With no pre-emphasis, the eye-opening varies from 268ps for the 4" backplane trace pair to 226 ps for the 24" backplane trace pair. At full (25%) pre-emphasis, the waveform for the 4" trace pair is significantly degraded while the 24" trace pair continues to benefit from the additional pre-emphasis.

Figure 12 is similar to Figure 11 except for backplane trace pair #13. Notice that unlike the data taken from backplane trace pair #2, the data eye-opening for the 16" and 24" backplane trace lengths continue to benefit from full pre-emphasis (25%).

Figure 11. Pair 2 Eye-Opening vs. Pre-Emphasis and Trace Length

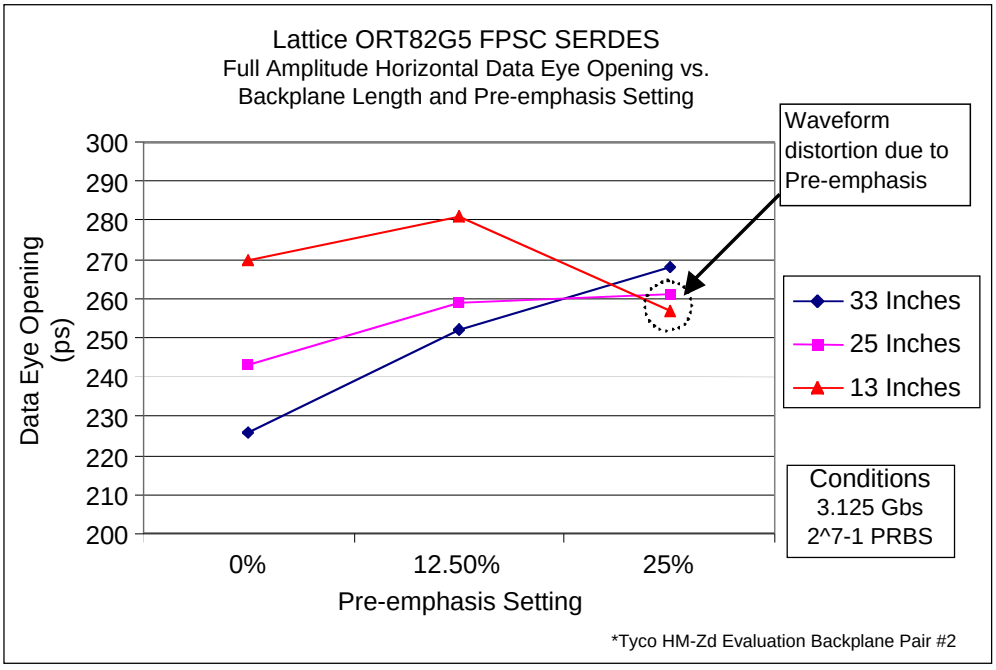
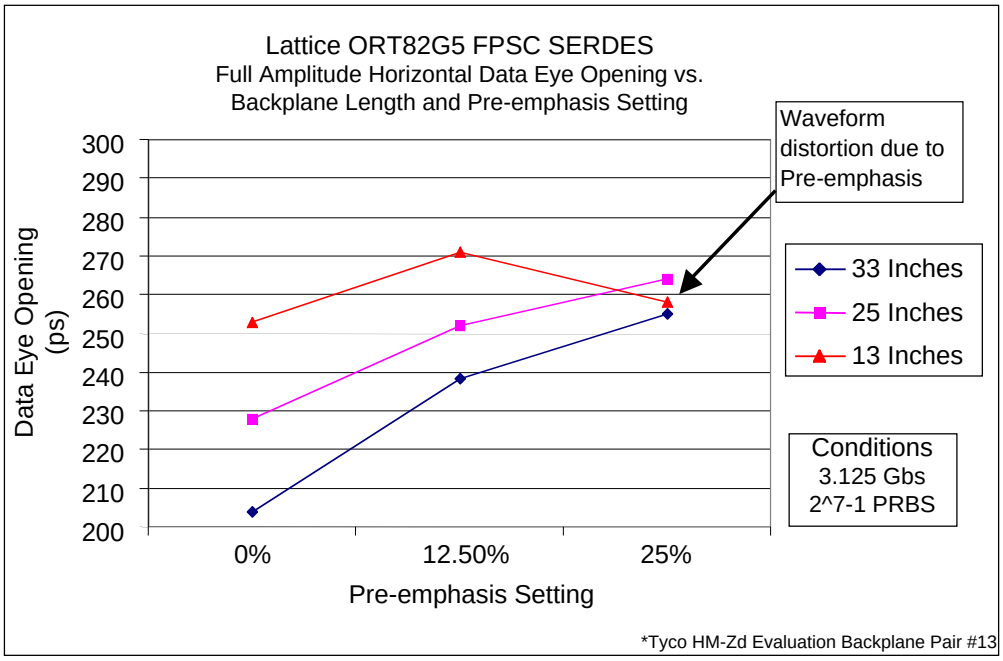


Figure 12. Pair 13 Eye-Opening vs. Pre-Emphasis and Trace Length



Data-Rate Experiment

Bit-error rate testing was performed across 16 and 30 inch backplane traces, at 25 and 125 degree C temperatures. The total PCB trace path length for this testing is 26 and 40 inches, when port card and ORT82G5 evaluation board traces are included. Supply voltage and operating speed were varied as indicated. The test criterion used was the observation of 1E12 data bits received with no bit-errors occurring. Detailed bit-error rate and jitter performance is beyond the scope of this application note. A detailed discussion of the ORT42G5 and ORT82G5 jitter and error-rate performance, can be found in another application note[2].

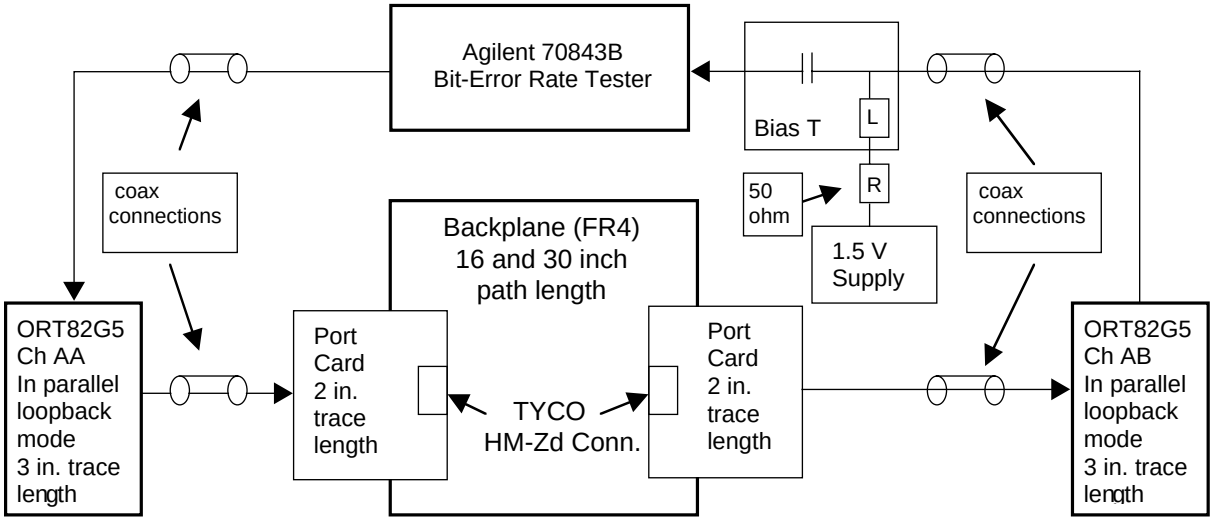
Test Equipment

– ORT82G5 evaluation board
– Tyco Electronics XAUI backplane with two port cards[1]
– Agilent 70843B Error Performance Analyzer
– HPE3630A, HPE3610A, HP6213A power supplies
– HP8656B clock source
– Temptronic Thermostream TP04100A-1
– PicoSecond 5575A Bias-T

Test Setup

The test configuration used to verify error-free operation is shown in Figure 13. High-speed ORT82G5 serial interface buffers are connected at both the Tx and Rx signal ends of the PCB signal path under test. Two separate SERDES channel in the ORT82G5 device were each placed in a parallel loopback mode of operation (with 8B/10B encoding/decoding disabled). The Agilent BERT was used to generate the data test pattern. Matched length 50 ohm coax cables used in the signal path were found to have minimal loss, as compared to PCB traces.

Figure 13. Bit-Error Rate Test Setup



Test Setup Parameters

– ORT82G5 680 PBGAM plastic ball grid array (wire-bond), -3 speed grade
– Ambient temperature = 25 to 125° C
– Data pattern = PRBS 2^7 - 1
– Power supply = 1.4V to 1.6V

PCB Specification

– The 2 inch PWB section (port card) is composed of 6 mil wide (1/2 oz. copper thickness) 100 Ohm differential impedance traces
– Backplane - 200 mils thick, 14 layers, Nelco 4000-6 FR4
– All signal layers are 10 mil wide (1/2 oz. copper thickness) traces designed for 100 Ohm differential impedance
– All signal layers buried and surrounded by GND planes
– Port Card - 93 mils thick, 14 layers, Nelco 4000-4 FR4

Data Summary

A small sampling of devices was tested over temperature and supply voltage variations. The maximum speed of operation was determined at each test condition. Results of the testing for the worst-case device are shown in Table 3 and Table 4.

Table 3. Bit-Error Rate Test Results with 26 Inch PCB Connection

VDSerdes	Temp	PE	Speed
1.60	25C	25%	4.1G
1.40	25C	25%	3.9G
1.60	125C	25%	3.8G
1.40	125C	25%	3.7G

Table 4. Bit-Error Rate Test Results with 40 Inch PCB Connection

VDSerdes	Temp	PE	Speed
1.60	25C	25%	3.5G
1.40	25C	25%	3.4G
1.60	125C	25%	3.3G
1.40	125C	25%	3.2G

Test criterion used for all tests was 1E-12 maximum bit-error rate.

Conclusion and Backplane Design Guidelines

The ORT42G5 and ORT82G5 FPSCs can support high-speed serial backplane interconnections over a broad range of data rates and connection path lengths. Measurement data presented in this document illustrates device performance over a typical backplane system, designed for high-speed serial interconnections. ORT42G5 and ORT82G5 (per channel) programmable power output levels and pre-emphasis levels, allow applications to optimize each signal interface.

The effectiveness of using pre-emphasis to compensate for the high-frequency losses of longer path lengths was shown in Sections 2 and 3. Eye-diagram measurements were found to be a very good indication of backplane interconnection performance. The specified 80mV minimum eye-opening criterion for the ORT42G5 and ORT82G5 was found to consistently predict error-free performance (less than 1E-12 error-rate) in all the measurements made.

Performance variations due to PCB layout/board-construction were measured in Section 3. It was shown that these variations can be significant, even between different layers within the same board. This illustrates the critical nature of hardware designs extending to multi-Gb/s interconnection rates.

High-speed interconnection performance in a system is dependent on many device, system and environment characteristics. For this reason it is not possible to specify performance limits that apply to all applications. Table 5 shows the ORT42G5 and ORT82G5 operating data rate limit for the fastest device speed grade.

Table 5. ORT42G5 and ORT82G5 FPSC Frequency Limit

Device Speed Grade	Max Data Rate
-3	3.7 Gb/s

This table takes into account variations in device speed, temperature, and supply voltage. The data of Section 4 is consistent with this table, for a speed grade -3 device, while operating over a 26 inch connection path, in the TYCO backplane test system. The maximum connection path length that an application can reliably use, is a complex system level question that the application designer must address.

The following suggestions are made, for ORT42G5 and ORT82G5 applications, to help achieve best interconnection performance results:

- Careful selection of backplane connectors and other components touching the high-speed path, is critical. Each component should be electrically characterized through the frequency range of operation. Pay close attention to the parasitic reactance parameters of these components.
- Great care should be taken in the port card and backplane PCB design to follow good high-speed design practices.
- Use analog simulation tools extensively. Analog interconnection circuit simulation is a valuable tool at the system design level. SPICE models of interface and connection devices, which are available from most vendors, can be used to assess signal integrity issues, prior to building models.
- Early laboratory measurements of the longer and/or more critical interconnection paths should be made to reduce technical risk, prior to full system model design. Eye-diagram and bit-error rate measurements are recommended. ORT42G5 and ORT82G5 SERDES I/O buffer HSPICE models are available.

References

1. Tyco Electronics XAUI Z-Pack HM-Zd Backplane Evaluation Test System (this system was selected by 10GEC as the XAUI interoperability standard)
2. SERDES Test-Chip Jitter Performance, Lattice Technical Note TN1032
3. ORCA® ORT42G5 and ORT82G5 Data Sheet

High-Speed PCB Design Considerations

April 2003 Technical Note TN1033

Introduction

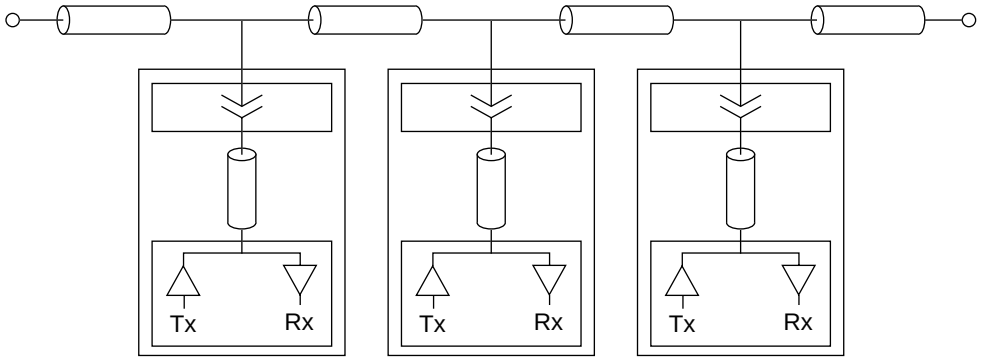
The backplane is the physical interconnection where typically all electrical modules of a system converge. Complex systems rely on the wires, traces, and connectors of the backplane to handle large amounts of data at high speeds. The communications between the various backplane modules depends on the inherent electrical characteristics such as impedance, capacitance, and inductance derived from connectors, trace lengths, vias, and termination, to name a few. An extremely important factor for a distributed-load, high performance backplane is a basic understanding of the design practices used to ensure good signal integrity.

This technical note examines some basic differences in interconnection topologies. It describes the various issues that should be considered while designing a backplane and focuses on the critical aspects of point-to-point transmission lines that are run through a backplane. These aspects include PCB line structure, vias, device packaging and backplane connectors. A PCB design checklist is provided to aid the designer. Some frequency specific discussion and guidelines are given. This document also discusses Lattice Semiconductor's FPSC product line and it's high-speed backplane interfaces. These provide serial streams up to 3.7 Gbps through CML differential buffers.

Backplane Topology and Overview

Three different system interconnection topologies are normally used in backplanes today. These are multi-point, multi-drop and point-to-point. Traditionally systems have used multi-point/ multi-drop connection topologies, which provided efficient interconnection and communication between multiple devices, with a single net (node), as shown in Figure 1.

Figure 1. Multi-Point Backplane Illustration



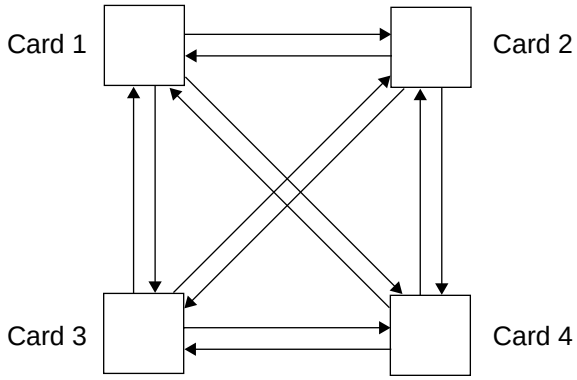
Unfortunately, this net structure provides serious data-rate limitations. Each net contains tees or branches at each point where the card connects to the backplane. These tees provide transmission line discontinuities and mismatches along the backplane signal path. The result is large signal reflections occur at every card to backplane interface. These reflections can propagate back and forth for substantial time periods and severely degrade signal integrity at higher speeds. Acceptable signal communication is normally achieved by waiting for the reflected signals to settle out, for each bit of transmitted data. This imposes significant speed limitations. For this reason multi-point and multi-drop backplane topologies generally have speed limits below 100 Mbps. This limit can easily drop below 10 Mbps as physical line lengths and the number of card slots increase.

The point-to-point interconnection topology eliminates the signal path branches described above. The resulting signal reflections are eliminated and maximum data rates are increased dramatically. This type of backplane interconnection can be used with data-rates to 3 Gbps and above, with careful design methods.

The disadvantage of this approach is an increase in the number of backplane nets and card port interfaces that may be needed. The single net connection between n cards, in a multi-point backplane, must be replaced with n(n-

1) unidirectional point-to-point links. Each card must provide n-1 transmit and n-1 receive ports for full system interconnectivity. As an example, a four PCB module system with full interconnectivity is shown in Figure 2.

Figure 2. Four Card Point-to-Point Interconnection System



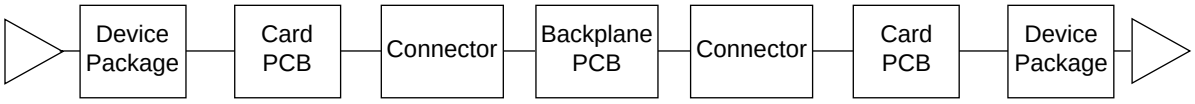
Each card must provide 3 transmitter and 3 receiver ports. Each arrowed line represents a point-to-point backplane net.

Recent communications equipment designs have shown a rapidly growing need for higher bandwidth interconnection between PCB modules. The fast evolving IC technology, with its multi-gigabit processing and driving capabilities, has made point-to-point backplane the topology of choice for many of today's new hardware systems. Both serial and parallel data structures can be supported with this topology. Lattice Semiconductor has introduced several IC products with multiple ports, each designed with Gbps backplane drive capability. These devices will be described later in this document. The remainder of this document will focus on PCB design aspects of the point-to-point backplane interconnection links.

Point-to-Point Backplane Signal Path Structure

The typical point-to-point topology utilizes a simple, single-path interconnection structure that extends from a transmitting device on one card, across a backplane and second card, to a receiving device on another card. The physical path for such an interconnection is illustrated in Figure 3.

Figure 3. Interconnection Link Physical Structure



The point-to-point interconnection elements are all serially connected and provide a single signal path. Each element may be thought of as a transmission line segment. Ideally, by controlling and matching the characteristic impedance of each line segment, a uniform electrical signal path is created. Signals can then propagate the entire path length with no reflections occurring. Adding a resistive termination at the receive device input, with value equal to the characteristic impedance of the line elements, would provide a distortionless data link with maximum bandwidth, between the transmit and receive devices.

Each of the elements in Figure 3 can be broken down into of a number of sub-elements. The PCB elements for example, which provide the more significant transmission line segments in the data path, consists of the sub-elements: metal traces, dielectric layers, ground plane layers, and (inter-layer) vias. Each of these sub-elements is a critical part of the signal path and can cause electrical line discontinuities and signal reflections, if not properly designed. The design aspects of the elements and sub-elements contained in Figure 3 will be discussed in the following sections.

Advantages of Differential Signaling

The inherent system advantages of differential signal interconnection schemes are well known in all fields of electronic design. These advantages are especially important in high bandwidth, high-density hardware systems where very low error-rate data links are required. Differential signaling provides critically needed immunity to common-mode electrical noise that is present at significant levels in most application systems. For example, using differential signaling avoids the classic "ground bounce" noise problem that is experienced with many high density ICs that use single-ended interfaces. It also provides higher noise margins, which lead to lower bit-error rates in digital data links. For these reasons, Lattice Semiconductors provides fully differential I/O interfaces, as will be described in the Device Introduction section. Differential signal interconnection methods should be used for all critical, high-speed interconnections.

Board Design Practices

Differential Trace Design

Differential signal trace-pairs with controlled impedance can be arranged in a number of different configurations. Most common are the following four figures.

Figure 4. Edge Coupled Microstrip (surface routing)

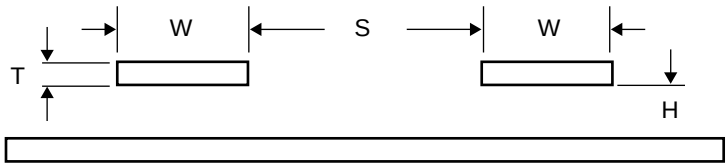


Figure 5. Edge Coupled Stripline (sandwiched between two reference planes)

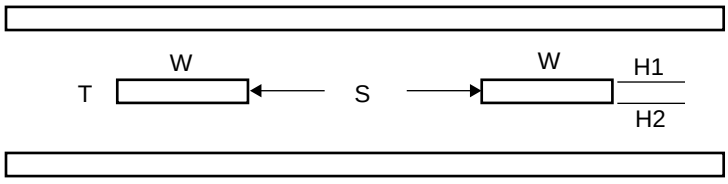


Figure 6. Offset Edge Coupled Stripline (same as Figure 5, but not centered between reference planes)

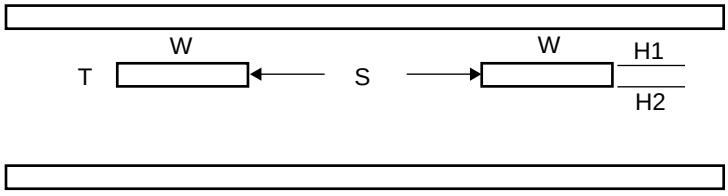
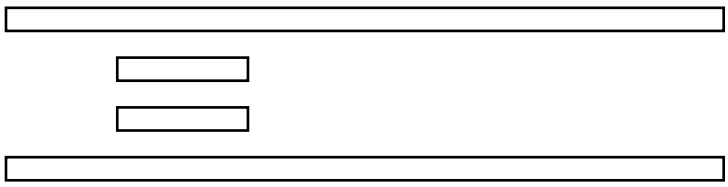


Figure 7. Broadside Coupled Stripline (also referred to as Dual Stripline)



100 ohm characteristic impedance has become an industry standard value for differential lines used for interconnection. This impedance level lends itself well to PCB structures and other components designs where controlled transmission line impedance must be provided.

A 100 ohm differential line can be constructed with two 50 ohm single-ended lines of equal length.

As the two line traces are brought near each other (as shown in Figure 4 through Figure 7), the field coupling between the traces reduces the differential mode impedance of the line. To maintain 100 ohm differential impedance, the trace width must be reduced slightly. As a result the common mode impedance of each trace in a 100 ohm couple-trace differential pair will be slightly less than 50 ohms.

Achieving a 100 ohm _differential impedance with a coupled pair of traces implies that the single ended impedance of Z0 ranges from 53 _to 60 ohm, with a coupling coefficient typically ranging from 1-15%. The relationship between the common mode impedance Z0 and the differential impedance Zdiff is given by the expression Zdiff = 2 Z0 (1 - kb)/(1 + kb), where k is the trace coupling coefficient.

50 ohm resistors, tied to ground, are normally used to terminate the 100 ohm differential lines. This provides the ideal differential line termination, which is most important since the data links use differential signals. The slight impedance mismatch that occurs in the common mode is usually of little consequence. Normally only noise and crosstalk signals occur in common mode.

Common Mode Noise Tolerance

In order to prevent common mode noise from converting to differential mode noise, it is important to maintain the symmetry of the differential pair. Reflections and impedance mismatch in the common mode will not affect the differential mode performance as long as the two modes can be kept relatively orthogonal.

The loop area is defined as the area between the signal path and its return path. On differential traces, the signal is on one trace and the return is on the other trace. So the loop area is a function of how close the traces are routed together. If we are concerned about EMI emission and susceptibility, which is generally understood as a loop area concern, we must route the traces close together. The more closely we route them to each other, the smaller the loop area will be and the less EMI will be generated.

One of the primary advantages of differential signals is the signal-to-noise ratio improvement that is obtained. Since the signal is one polarity on one trace and the other polarity on the other trace, the resulting signal at the receiving device is twice what the single-ended signal would be. Ideally common mode rejection at the receiving device is such that the receiving device only responds to the difference in signal level between the two traces. Since noise is typically in the common mode, it is rejected at the receiver and maintains a high differential signal-to-noise ratio.

In order to have good common mode noise rejection, it is important that any noise that is present affects the signals on both traces equally. That is, if noise is coupled into one trace, an equal amount of noise must be coupled into the other trace. Then the common mode rejection capability of the receiving circuit will reject the noise. But if noise is coupled into one trace more strongly than into the other trace, the noise will appear as a differential mode signal to the receiver and be amplified. The way to ensure that any noise is coupled equally into both traces is to route the two traces very close together. Then they will both be in the same noise environment.

PCB Trace Impedance Calculation

In the past, calculation of the characteristic impedance for a printed circuit board trace was a complex, error prone process involving complicated calculations and approximation. Nomographs and simplified formulas have been generated to simplify the design process, but are often inaccurate. The most accurate method available is a field solver program (usually 2D, sometimes 3D), which solves Maxwell's equations directly over the volume of PCB under consideration using finite elements. These simulations can be verified in hardware with a Time Domain Reflectometer (TDR) measurement device.

One example of a 2D field solver program is the Si6000b program from Polar Instruments[1]. This is available as a shareware evaluation version, and can be downloaded for evaluation and testing on a workstation.

Even using a field solver, there are still uncertainties in the impedance calculation arising from variations in the effective dielectric constant in the glass fiber, prepreg, and epoxy used in typical FR4 manufacturing. The average

dielectric constant of FR4 varies from 4.2 to 4.5, depending on the material, exact location, and construction methods used.

Verification of the impedance on a PCB depends on actual measurements of typical copper traces. Some manufacturers use an auxiliary test section of a PCB called a coupon, which is a long rectangular test section of PCB with pads designed to accept probes from a TDR measuring instrument. It is not unknown for manufacturing errors to result in over-etching of the copper traces, with a resultant impedance error. Monitoring production quality with coupons can prevent this type of problem.

Examples of PCB Trace Impedance Calculation

As a calculation example, we will find the differential impedance for a pair of 6 mil traces in 1/2 ounce copper with 10 mil spacing that is on an FR4 substrate with a spacing of 5 mils above the ground plane (microstrip). The copper thickness (T) is 0.7 mils. Figure 8 shows the parameters. Note that this example uses a predecessor to the Polar Si6000b transmission line calculator product mentioned previously.

Figure 8. Differential Microstrip example with Polar CITS25 Impedance Calculator Tool

In a typical FR4 PCB, there will be three types of differential pair routing encountered. For connections to surface mounted components, edge coupled microstrips may be needed, while connections between through-hole components or via pairs can use stripline and offset stripline. Dual stripline with broadside coupling should be avoided, since this configuration is subject to differential noise coupling from the reference planes. Another problem with broadside coupling is that any asymmetry in the PCB manufacturing can result in an asymmetric trace impedance, causing mismatch in the effective electrical length, even if the physical lengths match exactly. Using edge coupled differential pairs; it is easier to maintain symmetry.

Vias, connectors, and component pads all introduce impedance discontinuities into the signal path, and this can be measured with TDR techniques.

In order to avoid crosstalk, when laying out differential pair trace with spacing of value S, it is recommended to place pairs no closer than a distance of 3 S, and preferably a distance of 4 S if possible. This rule can be relaxed if a differential pair is only briefly in proximity with another pair, such as at a connector or via layer switch.

PCB Design Checklist

1. Use 100 ohm_ differential impedance pairs on PCB. Controlled impedance lines should be specified in PCB manufacture.
2. Match trace lengths in a pair with tolerance of 20% of the signal rise/fall time.
3. Use connectors that are designed and characterized at the highest data frequency. (Vendors should provide characterization and model data.)

4. Use stripline construction with ground/VDD planes above and below the differential pairs.

5. Use edge-coupled pairs in PCBs; try to avoid broadside coupled pairs.

6. Use 3 S separation rules between pairs to avoid crosstalk and excess coupling. Use offset stripline routing to get higher density of differential pairs with each routing layer running orthogonal to each other.

PCB Layer Design (Board Stack-up)

Multi-layer boards are a must in both daughter board and backplane design. The multiple metal layers facilitate high connection density, minimum crosstalk, and good ElectroMagnetic Compatibility (EMC). These factors are key to achieving good signal integrity for all the signal interconnections. Ideally, all signal layers should be separated from each other by ground or power planes (metal layers). This minimizes crosstalk and provides homogeneous transmission lines, with properly controlled characteristic impedance, between devices and other board components. Best performance is obtained when using dedicated ground and power plane layers that are continuous across the entire board area. When it is not feasible to provide ground or power planes between signal layers, great care must be taken to ensure signal line coupling is minimized. Orthogonal routing on adjacent signal layers minimizes coupling and should be used. CAD tools, which predict line coupling and signal crosstalk, can be very helpful in this type of design.

Vias

Vias generally provide two purposes. One is used for mounting a through-hole component to a board. The second is to interconnect traces on different metal layers. Electrically, vias are often modeled as having an inductive and capacitive parasitic value. Smaller vias have lower capacitance. Short length, larger diameter vias have lower inductance. Both parasitic elements can have detrimental affects, but it is often the inductance parasitic element that provides an unexpected series impedance that creates problems.

Lattice High-Speed I/O Offerings

Lattice Semiconductor has introduced a series of silicon devices utilizing high-speed CML and LVDS serial interfaces that feature clock synthesis to embed data and clock in a serial stream in the transmitter monolithic clock and data recovery in the device receiver. These devices are listed in the following table.

Table 1. Lattice Semiconductor ORCA FPGA, FPSC, ispXPGA and ispGDX2 High-Speed I/O Devices

Device	Description
OR4E02/04/06	FPGA Family with high-speed differential I/Os
ORLI10G	10 Gbps Line interface FPSC
ORT8850H/L	6.8 Gbps Backplane FPSC (850 Mbps/ch)
ORT82G5	29.6 Gbps Backplane FPSC (3.7 Gbps/ch)
ORT42G5	14.8 Gbps Backplane FPSC (3.7 Gbps/ch)
ORSO82G5	21.6 Gbps SONET Backplane FPSC (2.7 Gbps/ch)
ORSO42G5	10.8 Gbps SONET Backplane FPSC (2.7 Gbps/ch)
ispXPGA	17 Gbps with SERDES FPGA (850 Mbps/ch)
ispGDX2	13.6 Gbps with SERDES (850 Mbps/ch), 38 Gbps without SERDES

The ORT8850H/L, ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 have integrated serializer and deserializer with CDR (Clock & Data Recovery) blocks, and also feature de-skew FIFO's that remove skew between multiple serial channels. This facilitates bonding of multiple serial channels for synchronized gigabit data transfers between chips, boards, racks, and systems. The data format is either SONET, with a subset of the full GR253 standard supported, or 8b/10b coding. The ORT82G5 and ORT42G5 support eight or four channels of serial data at rates up to 3.7 Gbps (2.96 Gbps per channel after 8b/10b decoding). The ORSO82G5 and ORSO42G5 support eight or four channels of serial data at rates up to 2.7 Gbps. At these high speeds Current Mode Logic (CML) I/O buffers are used.

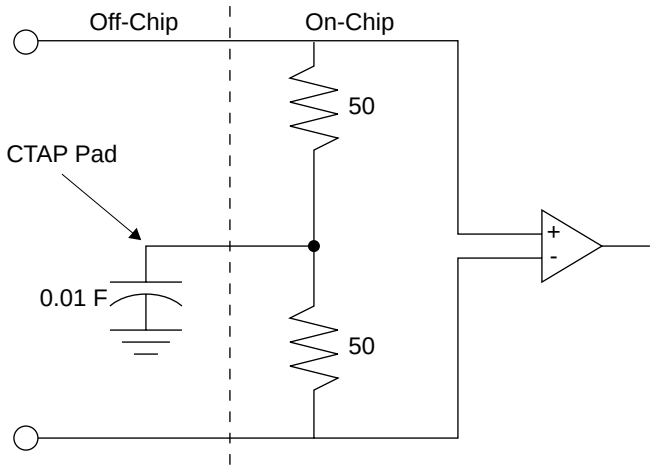
The ORLI10G provides a simpler high speed interface of 16 LVDS channels, without CDR or skew compensation. A synchronous, forward clocked interface can be used, with rates up to 850 Mbps. Great care must be taken by system designers to insure interconnection skews are properly controlled. This may impose speed and/or interconnection distance limits in some applications.

The ispXPGA and ispGDX2 also have embedded SERDES blocks with CDR circuits. Both families support 8b/10b, 10b/12b and Source Synchronous mode. The encoding and decoding of 8b/10b blocks are not implemented in these devices.

Integrated Input Terminations

Lattice devices with high-speed serial CML and LVDS inputs provide built in, programmable, 100 ohm differential line termination resistors. Integrating these resistors on-chip is very important in high-density packaging such as ball-grid arrays where an on-board resistor cannot be placed close to the device inputs, off-chip resistors significantly reduce performance and increase the effects of reflections. Lattice differential input terminations include center-tap access. The ORT8850 input, for example, is shown in Figure 9.

Figure 9. LVDS Receiver Termination



The center-tap is a virtual ground which may be ac-coupled to ground to increase receiver common mode noise immunity, as shown in the figure. Embedded LVDS output buffers also have on-chip 100 ohm_ differential terminations, but do not have a center tap. These terminations have been shown to reduce near-end crosstalk significantly.

ORCA Series 4 FPGAs and the programmable I/O buffers on the FPSCs, including the ORT8850H/L, ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 also include special programmable LVDS drivers and receivers. This type of termination scheme is also available on the Series 4 general purpose FPGAs. These LVDS I/Os also include driver and receiver on-board 100 ohm _termination, but without the center tap. This termination resistor can also be disabled at the LVDS pair level. This scheme works well for receiver termination on a pin-by-pin basis, however it is programmable and can be implemented on the transmitters (drivers) also, thereby extending the reach of the LVDS signaling.

ispXPGA and ispGDX2 Family devices do not provide internal input termination resistors and require external termination at receiver inputs.

Special Design Considerations at 622/850 Mbps

Line Loss and Impedance Discontinuities

At data rates of 622 Mbits and higher, it should be realized that the skin effect is extremely important for signal conduction. Small traces on a PCB (like 4 or 5 mil widths) will exhibit significant signal attenuation over long distances. Over-etching of a PCB can produce narrow traces that can reduce the signal amplitude available at the receiver.

The end result is that, to the designer, the interconnection between devices resembles a badly designed low pass filter, with attenuation, which increases with frequency. For this reason, the longer the backplane, the wider the signal traces should be made. Long backplane traces (more than 20 in.) should have trace widths of 10 or 12 mils.

Connectors and vias in the signal path introduce discontinuities that resemble lumped elements in an electrical model. One way to take this into account is to perform SPICE simulation of the backplane system using lossy transmission line models, and manufacturer supplied models of the connectors, signal drivers, and signal receivers.

High-Speed Connectors

Many connectors have been tried and discarded in high-speed applications. Surprisingly, some out-dated connector designs have been found to be usable at gigabit data rates. An example of this is the venerable DB-9 connector, which is sometimes found in Fibre Channel products. A more modern approach is to use controlled impedance connectors specifically designed for high-speed data, where abundant ground connections and shielding features reduce the noise and impedance discontinuities seen in older connectors.

Examples of these are the AMP Mictor connectors, and the 2mm standard backplane connector families that are available from various suppliers for the 2 mm hard metric backplane standard (such as the AMP HS3 connector). These are available in both vertical and horizontal configurations. Several evaluation cards use an unshielded 2 mm connector (AMP 636120-1), and this provides good performance for driving twinax cables up to a distance of 65 ft (at 622 Mbps), error free.

Device Packaging

Transmitter and receiver device packaging parasitic reactances are important to signal integrity. Wire-bond and package substrate inductance and capacitance should be included in device SPICE models. Simulation of package parasitics has shown that impedance transformation and signal reflections can result at higher frequencies. Pin location in larger packages can have a significant impact on the parasitic values of the model. Internal receiving device terminations, such as provided in Lattice LVDS and CML buffers, were found to have superior performance when compared to receivers which require external resistor termination components.

High-Speed Copper Cables

High-performance cables generally far outperform PCB interconnections in terms of bandwidth and signal attenuation. This is because a high-performance cable uses expanded Teflon dielectric (PTFE); silver-plated conductors, and low-loss shielding material. These cables are also engineered with a conductor geometry that is usually extremely close to the optimal position for the desired bandwidth and characteristic impedance.

One cable that performs extremely well is the W. L. Gore DXSN2112 Eye-opener Plus cable. This high performance cable is engineered specifically for data transmission at 622 Mbps. Unfortunately, this cable is not easily assembled with connectors using simple hand tools. Complete cables with connectors may be ordered directly from Gore. The cable assembly that matches the 2 mm backplane connector (AMP 636120- 1) on many Lattice evaluation cards is Gore part number 2MMA3106.

Another cabling example is included with the Lattice ORT8850 evaluation boards. In this case, connections through a path including dipswitches, backplane connector and 65 ft of Gore DXSN2112 cable were error free at 622 Mbps. When routing the signal through Motorola LVPECL buffers and receivers with Gore DXN2151 cable, this was seen to be error free at a distance of up to 90 ft. Minimal reductions in the distances are expected at the maximum 850 Mbps for the ORT8850.

Caution: Do not attempt to use Cat-5 or Cat-6 Ethernet cable. This cable is not designed for high-speed applications.

Special Design Considerations at 2.5/3.125/3.7 Gbps

At 2.5/3.125/3.7 Gbps, the design problem becomes substantially more difficult. The higher copper and dielectric losses occurring at these frequencies, generally limit PCB interconnection lengths to about 40 inches. The greatest care in all aspects of PCB layer and layout design is required at these frequencies.

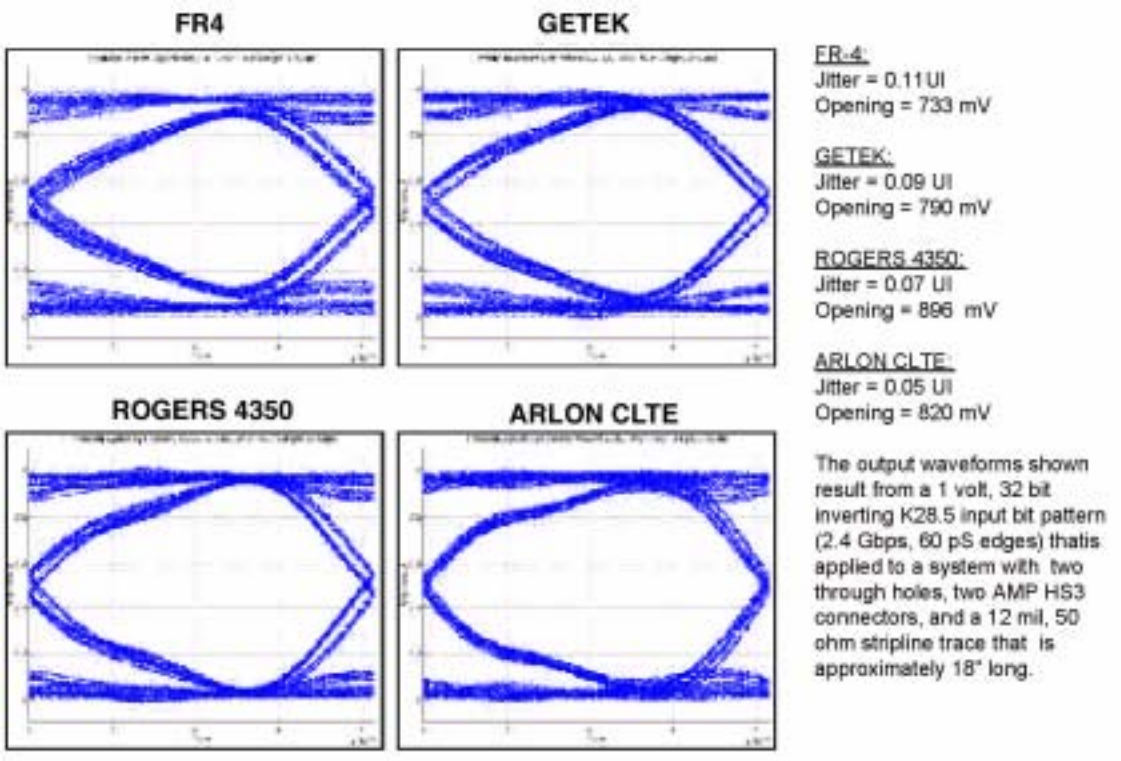
Board Thickness and Vias

Backplane thickness and via design can have significant affects on signal integrity. A backplane thickness of less than 0.200 inches generally gives the best results. Vias used to interconnect between layers create transmission line discontinuities. PCB designs with high-speed signal traces should be routed on as few layers as possible, thus limiting the number of vias. Thicker boards normally have longer length vias that can cause larger discontinuities, and degrade the signals. Longer vias connecting signal layers that are close together will appear as transmission line stubs, attached to the signal path. Stubs have been shown to have a very detrimental affect on signal integrity. Buried vias can be used to reduce this problem in thicker boards, but manufacturing costs for this technology can be prohibitive. Ideally, each signal path through the backplane should be kept on the same layer.

Board Material

FR4 dielectric loss becomes a significant design factor above 2 Gbps. Another design option is to use low-loss dielectric PCB material, such as Rogers 4350, GETEK, or ARLON. This is approximately double the cost of FR4 PCB material, but can provide increased eye-opening performance when longer trace interconnections are required; as shown from data collected by AMP Inc. Figure 10 gauges the improvement in signal eye opening at 2.4 Gbps, as lower loss materials are used. It can be seen from the figure that FR-4 material may deliver a satisfactory eye opening. It might then be the preferred low cost solution for a particular application.

Figure 10. System Eye Patterns (2.4Gbs) vs. PCB Dielectric Material



High-Speed Connectors and IC Packaging

Above 1 Gbps, connectors specifically designed for higher frequencies are recommended. Several new controlled impedance backplane connectors have become available, with data-rate capabilities in excess of 3 Gbps. A popular example is the Tyco Z-Pack HD-Zd 2-mm pitch family, which has been carefully characterized and modeled at frequencies up to 5 GHz. This class of connector provides some additional shielding benefits, which can aid the designer in controlling system noise and crosstalk.

The IC packaging comments of the previous section apply here as well. SPICE modeling of the package parasitics is the best way to evaluate effects on system performance, since measurement probes typically have parasitics equal to or greater than the packages used today. Care should be taken to insure that the vendor provided package models are valid through the intended frequency of operation.

Pre-Emphasis

Signal pre-emphasis is a means of compensating for the increased PCB loss that occurs at higher frequencies. A simple algorithm can be employed in the line driver to increase transmitted signal amplitude, whenever the data patterns have transitions (and therefore higher frequency content). This function is provided by the ORT82G5 SERDES CML drivers [4].

For longer PCB interconnection trace lengths, a significant increase in eye opening often results [3]. Use of the pre-emphasis can extend the maximum useable interconnection length, or allow the use of lower cost (greater loss) material and components, in system design. A more detailed description of the pre-emphasis feature may be found in Reference [4].

Conclusion

PCB backplane interconnections with serial data rates up to 3.7 Gbps are possible with today's technology. Lattice FPSC devices allow easy system design at rates to 850 Mbps through the ORT8850H/L serial or ORLI10G parallel interface. Increased performance with rates up to 3.7 Gbps is achievable with the ORT82G5, but greater care is needed in the PCB design. Systems running at these higher data rates may benefit from the use of transmitter pre-emphasis, controlled impedance connectors, and low loss PCB dielectric materials.

References

1. Si6000b field solving impedance calculator (downloadable demo version): http://www.polarinstruments.com/

2. W.L. Gore high-performance interconnect products: http://goreelectronics.com/

3. ORT82G5 High Speed Backplane Measurements, Lattice Tech Note TN1027

4. ORCA ORT82G5 and ORT42G5 Data Sheet

5. ORCA ORSO82G5 and ORSO42G5 Data Sheet

FPSC SERDES CML Buffer Interface

April 2003 Technical Note TN1029

Introduction

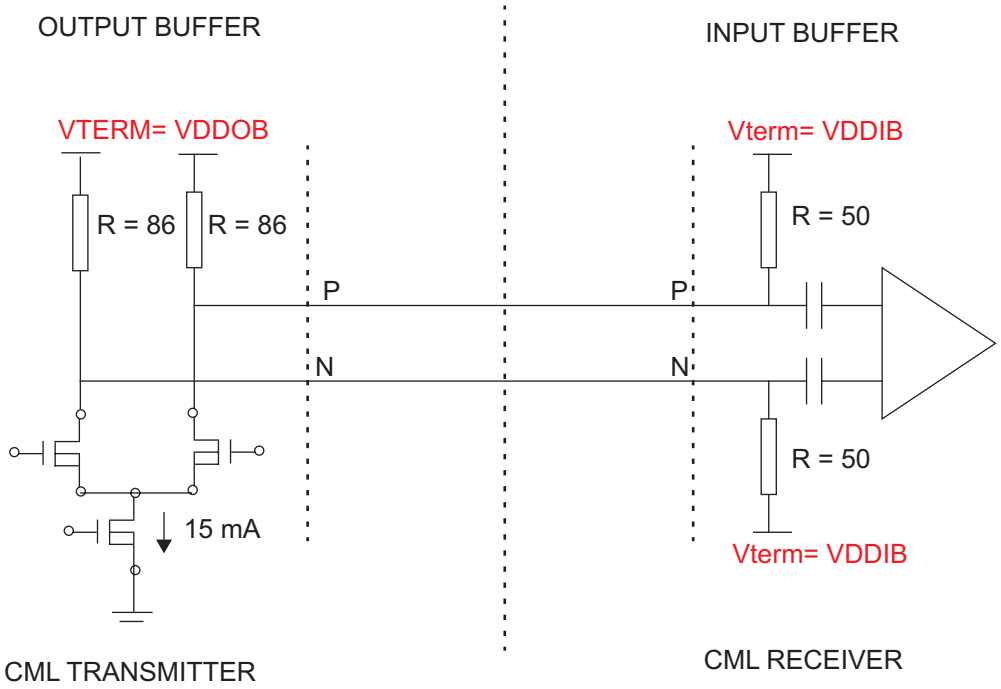
This document discusses the high-speed serial buffers provided in Lattice's ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 FPSC devices. These current mode logic (CML) buffers are part of a second generation Quad SERDES macrocell design and provide the high-speed (1.0 to 3.7Gbps) serial data input and output ports. The data sheet description of this device can be found in Reference 1. Portions of this data sheet are included in this document. Off-chip signal interface design and characteristics are the focus of this document. Interfacing to external high-speed devices with LVDS and LVPECL ports is also discussed. Transmission line interconnections between devices are required because of the high data rates. Practical considerations related to printed circuit boards, cables and connectors that carry these signals are also touched on in this document.

CML Buffer Description

The SERDES macro uses 0.16 µm technology (0.16 µm drawn, 0.135 µm physical). Internal input and output terminations are provided to simplify board level interfacing for the user. A simplified schematic of the serial input and output buffers are shown below in Figure 1. The termination resistors and coupling capacitors are internal to the macro.

The SERDES macrocell provides separate Rx and Tx power input nodes VDDIB and VDDOB for each channel, allowing the receiver input termination and transmitter output termination to be biased at different level, independent of the core VDD voltage (1.5V).

Figure 1. SERDES CML Buffer Schematic Diagram.



Interface Parameter Specification

The high operational speed of the SERDES serial I/O makes understanding the interface parameters especially important to the user. Proper interpretation of the parameters is needed for successful integration within a system. Signal interconnection performance, reliability and integrity are closely tied to these characteristics and their variational limits. This section attempts to summarize and discuss critical serial buffer interface parameters.

Correctly specifying the buffer I/O is a complex process. Methods used include extensive SPICE simulation and laboratory measurements. The official specification listing for the SERDES should be obtained from the Device data sheet (Reference 1). Revised issues of these documents will reflect updates and refinements in buffer specifications, as they are determined.

Input Buffer

Table 1 describes input buffer parameters and characteristics that are needed for application interface to other printed wiring board devices.

Table 1. Rx Input Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_j	Operating Junction Temperature		-40	-	125	°C
R_i	Internal Buffer Termination Resistance	Each input, to VDDIB	40	50	60	Ω
	Differential return loss	Package dependent	-	-	-	db
	Common-mode return loss	Package dependent	-	-	-	db
VDDIB	Input Termination Supply Voltage	Externally supplied	0	1.5 /1.8	1.9	V
V_i	Peak Input Voltage Limits		-0.3	-	VDD +0.3	V
	Common-mode Noise Tolerance	VDDIB bias dependent	TBD	-	-	V
	Internal Input ac-Coupling Time Constant		-	1.4	-	µS
	Clock and data recovery (CDR) closed loop bandwidth		-	3	-	MHz

Figure 2. Receive Data Eye-Diagram Template (Differential)

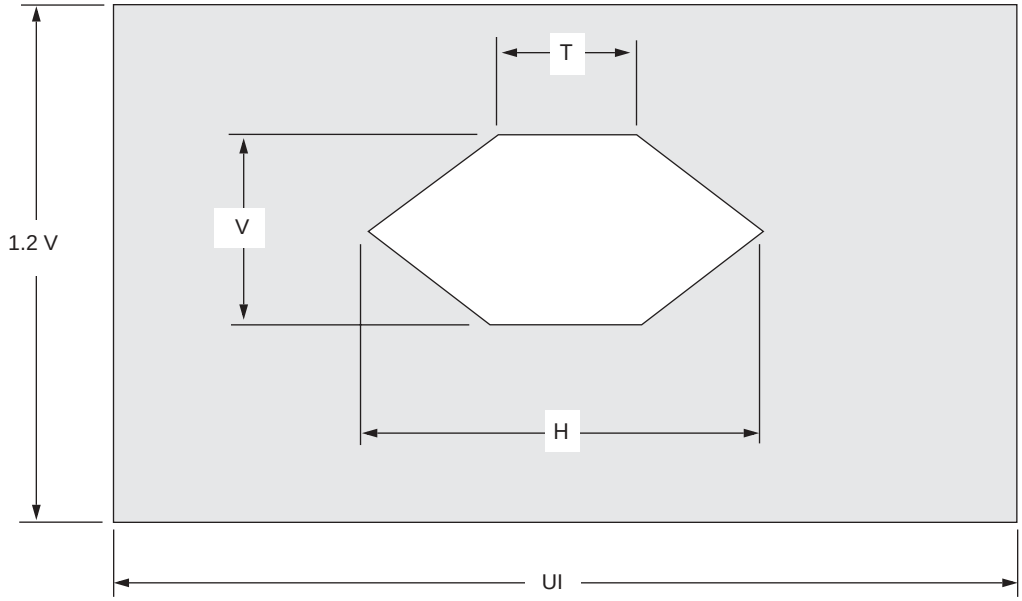


Figure 2 provides an eye mask characterization of the SERDES receiver input. The eye-mask is specified in Table 2 for two different eye-mask heights. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance. Almost all detrimental characteristics of trnasmit signal and the interconnection link design result in eye-closure. This, combined with the eye-opening limitations of the line receiver, can provide a good indication of a link's ability to transfer data error-free.

Table 2. Receiver Eye-Mask Specifications[1]

Parameter	Conditions	Value	Unit
Input Data			
Eye Opening Width (H)@ 3.125Gbps	V=175 mV diff[1]	0.55	UIP-P
Eye Opening Width (T)@ 3.125Gbps	V=175 mV diff[1]	0.15	UIP-P
Eye Opening Width (H)@ 3.125Gbps	V=600 mV diff[1]	0.35	UIP-P
Eye Opening Width (T)@ 3.125Gbps	V=600 mV diff[1]	0.10	UIP-P
Eye Opening Width (H)@ 2.5Gbps	V=175 mV diff[1]	0.42	UIP-P
Eye Opening Width (T)@ 2.5Gbps	V=175 mV diff[1]	0.15	UIP-P
Eye Opening Width (H)@ 2.5Gbps	V=600 mV diff[1]	0.33	UIP-P
Eye Opening Width (T)@ 2.5Gbps	V=600 mV diff[1]	0.10	UIP-P

1. With PRBS 2^7-1 data pattern, 10 MHz sinusoidal jitter, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., T_A = 0°C to 85°C, 1.425 V to 1.575 V supply, socketed device.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristic of the clock and data recovery (CDR) portion of the SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth (estimated to be about 3 MHz). For signals with high levels of low frequency jitter the receiver can correctly detect an incoming data stream, even with eye-openings significant less than that of Figure 2. This phenomenon has been observed in the laboratory.

Eye-diagram measurement and simulation are excellent tools of design. They are both highly recommended when designing serial link interconnections and evaluating system signal integrity.

Output Buffer

Table 3 describes output buffer parameters and characteristics that are needed for application interface to other printed wiring board devices.

Table 3. Tx Output Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_j	Operating Junction Temperature		-40	-	125	°C
VDDOB	Output Termination Supply Voltage	Externally supplied	1.3	1.5 /1.8	1.9	V
R_O	Internal Buffer Termination Resistance	Internally tied to VDDOB	69	86	103	Ω
R_L	Preferred external load	Terminated to 1.5V/1.8V	-	50	-	W
	Differential peak-to-peak output	Full-amplitude mode Half-amplitude mode	0.8 0.4	1.0 0.5	1.2 0.6	V
V_{OH}	Output voltage - High	VDDOB = 1.5V, 50Ω ext. load to 1.5V VDDOB = 1.8V, 50Ω ext. load to 1.8V	-	1.5 1.8	-	V
V_{OL}	Output voltage - Low	VDDOB = 1.5V, 50Ω ext. load to 1.5V VDDOB = 1.8V, 50Ω ext. load to 1.8V	-	1.0 1.3	-	V
t_r/t_f	Rise and fall time (20% - 80%)	Preferred ext. load (R_L)	50	-	110	pS
	Differential output skew	Preferred ext. load (R_L)	-5	-	+5	pS
	Pre-Emphasis amplitude	Low mode High mode	-	+12.5 +25	-	%

The CML outputs are designed to avoid damage with inadvertent short-circuit connections to ground and VDD.

External Interface

The SERDES high-speed serial buffers were optimized to interface externally to other similar buffers. Direct interconnection of Lattice SERDES buffers requires no external devices or components at the PCB level. Interconnection to other vendor's CML buffers is possible, but may require the addition of some passive components.

All interconnection circuits described in this section should use match length pairs of 50 ohm transmission line. Each will provide characteristic impedance termination of the line to provide maximum signal bandwidth. 50 ohms, an industry standard, provides maximum compatibility and suits present printed wiring board technology interconnections well, for circuit pack and backplane applications. It is also consistent with 100 ohm balanced transmission line interfaces which are becoming popular for high bandwidth shielded pair cable connections.

LVDS Device Interface

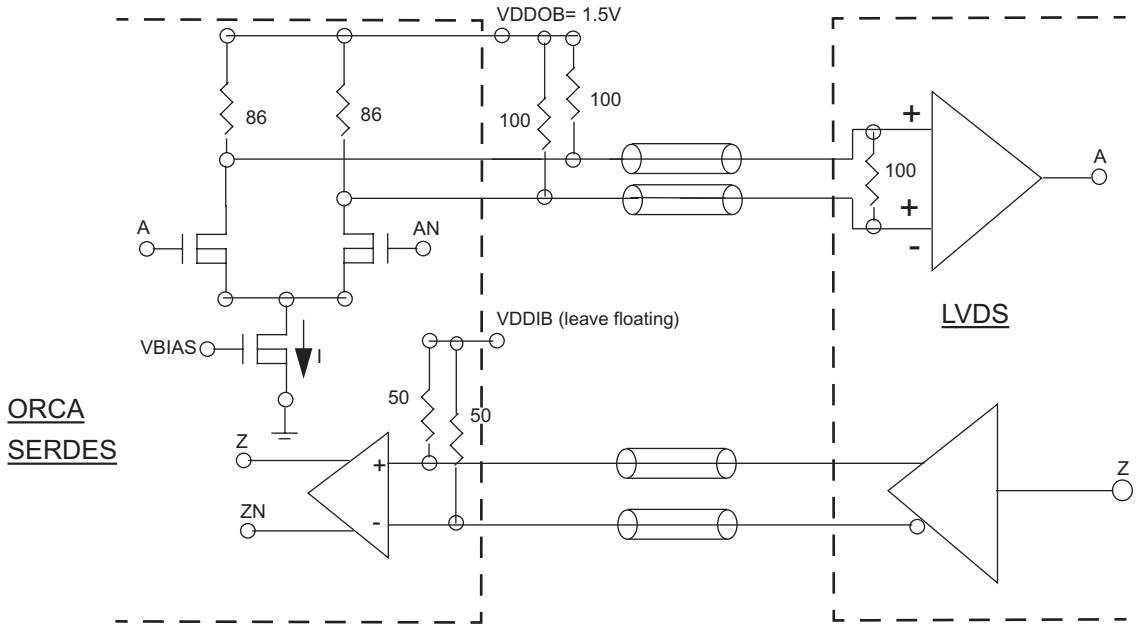
LVDS, like CML is intended for low-voltage differential signal point-to-point transmission (Reference 3). Many commercial LVDS devices provide internal 100 ohm input terminations. They are thus intended for use with 100 ohm characteristic impedance transmission line connections. Standard LVDS is specified with about 3 mA signal current which translates to a nominal signal voltage of 600 mVp-p (differential). Low power LVDS provides about 2 mA signal current. LVDS input and output parameters are shown in Table 4, as specified in the LVDS Standard.

Table 4. LVDS Parameters

Symbol	Parameter	Conditions	Min	Max	Units
Driver Specifications					
Voh	Output voltage high	Rload (dif)=100 ohm	-	1475	mV
Vol	Output voltage low	Rload (dif)=100 ohm	925	-	mV
|Vod|	Output differential voltage	Rload (dif)=100 ohm	250	400	mV
Ro	Output impedance, single ended	Vcm=1.0V to 1.4V	40	140	ohm
Receiver Specifications					
Vi	Input voltage range		0	2400	mV
Vidth	Input differential threshold		-100	+100	mV
Vhyst	Input differential hysteresis		25	-	mV
Rin	Receiver differential input impedance		90	110	ohm

Table 4 shows that LVDS devices have some degree of signal voltage range overlap with SERDES. Both use internal 100 ohm differential terminations at the receiver port. A direct interconnection of the two technologies, as shown in Figure 3, is therefore possible.

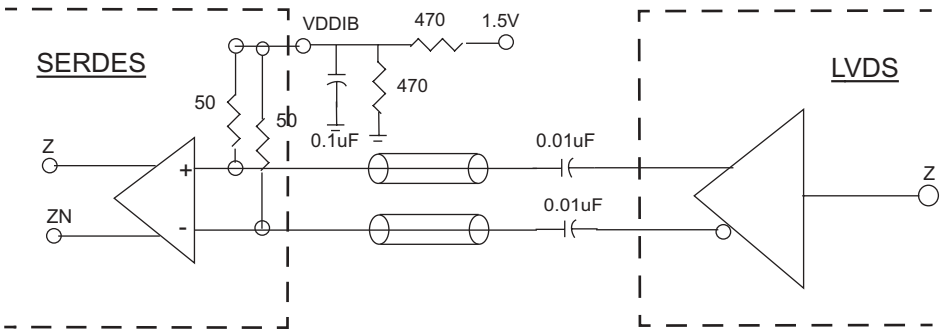
Figure 3. DC-Coupled SERDES CML to LVDS Interface



Within LVDS receivers, an internal input differential termination, of value 100 ohms, is typically provided. This termination resistor is usually floating with respect to ground. In the SERDES receiver the differential input termination resistor is center-tapped and biased to a voltage equal to 1.5V or 1.8V. This is required for proper operation of the output buffer. To properly drive the LVDS input from the SERDES output an external 100 ohm resistor to VDDOB is required on each output, as shown in Figure 3. Some LVDS devices provide a center-tapped input termination resistor, internally. If this center-tap is accessible, a capacitor to ground can be added to provide an additional level of immunity to system level common-mode noise.

In the LVDS to SERDES direction (lower portion of Figure 3), a floating input termination resistor may be provided by leaving the SERDES VDDIB pin floating. This provides a signal at the receiver input with a nominal common mode voltage of 1.2V. The maximum voltage swing at each input is +/- 200 mV. This is within the acceptable input voltage range of the receiver. A simple direct interface like this can be used in many applications. Higher common mode noise tolerance may be achieved with alternate ac-coupled LVDS driver to SERDES receiver connection, as shown in Figure 4.

Figure 4. AC Coupled LVDS to SERDES Scheme



The signal coupling capacitors and resistive voltage divider circuit is added to translate the LVDS output signal to the center of the SERDES input voltage range. This will increase the receiver tolerance to common-mode input noise voltage, and provide a higher tolerance range to common-mode and system and ground noise. Note that nominal resistor and capacitor values are shown in Figure 3 and Figure 4. Optimum values will vary in each application.

Analog simulation of interface circuits can be a very useful part of the design process. As a simple example, the SERDES to LVDS interface portion of Figure 5 is simulated, using the HSPICE models for the SERDES output buffer that is available from Lattice. Two 50 ohm ideal transmission lines of matched length were provided between the SERDES output and the LVDS input, representing PCB traces. Figure 5 shows the resulting signal voltage waveforms at the LVDS device input terminals, as predicted by simulation. Device package parasitic-elements were included. The P and N input common-mode (single-ended) and differential mode waveforms are shown. A random-digital signal pattern was used in the simulation to drive the SERDES buffer. Other parameters and conditions assumed were nominal IC processing parameters, nominal supply voltage and room temperature. Figure 5 shows a well behaved differential signal that should be an adequate LVDS input signal.

Figure 5. SERDES to LVDS Signal Simulation - Nominal Case

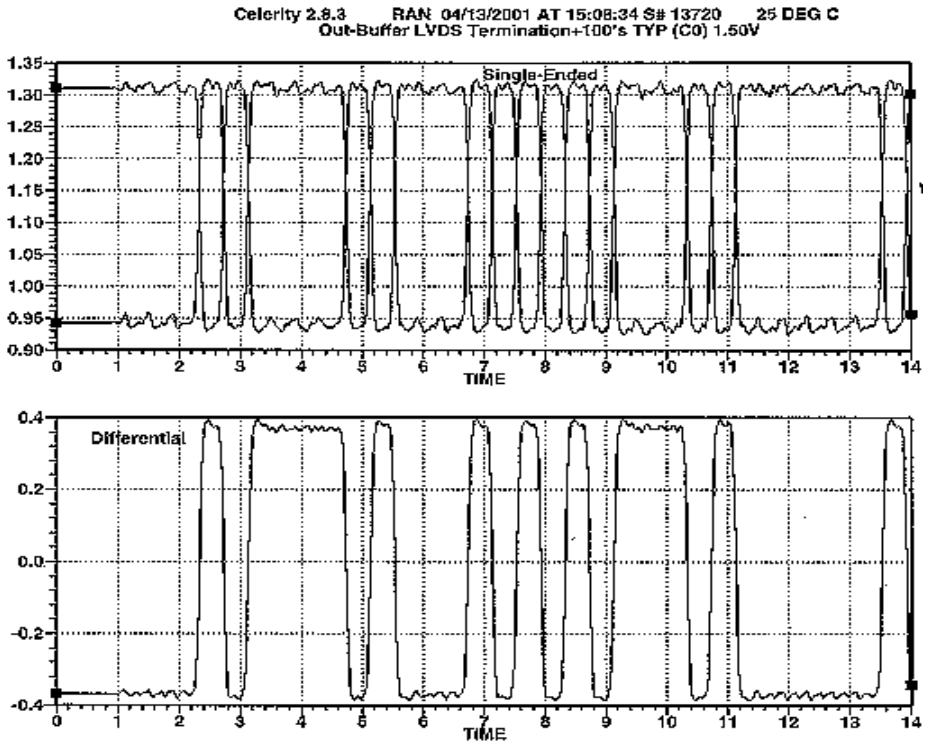
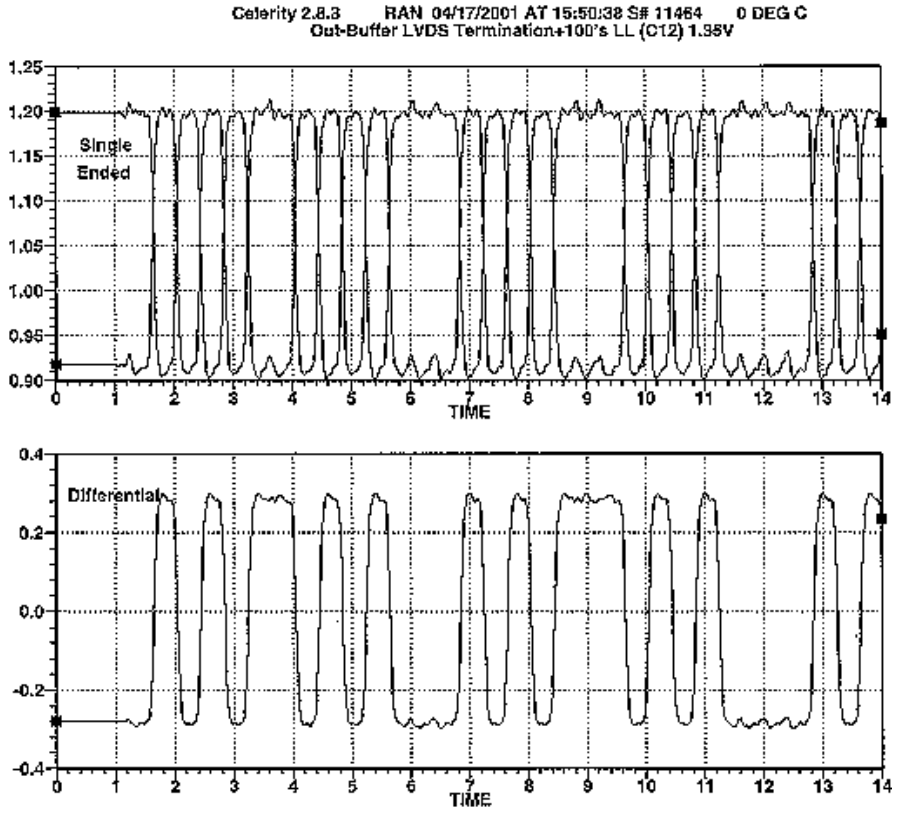


Figure 6 repeats the simulation of Figure 5, but under some worst case conditions. Extreme IC process parameters, low supply voltage, and 0 degree C temperature were assumed. The resulting waveforms in Figure 5 and Figure 6 are well within the acceptable operating range of a typical LVDS device. One of the important functions of circuit simulation is to verify correct operation while varying parameters and operating conditions over the expected range of variation.

Figure 6. SERDES to LVDS Signal Simulation - Worst Case



Low Voltage PECL Interface

Parameters for a typical LVPECL I/O device are listed in Table 5.

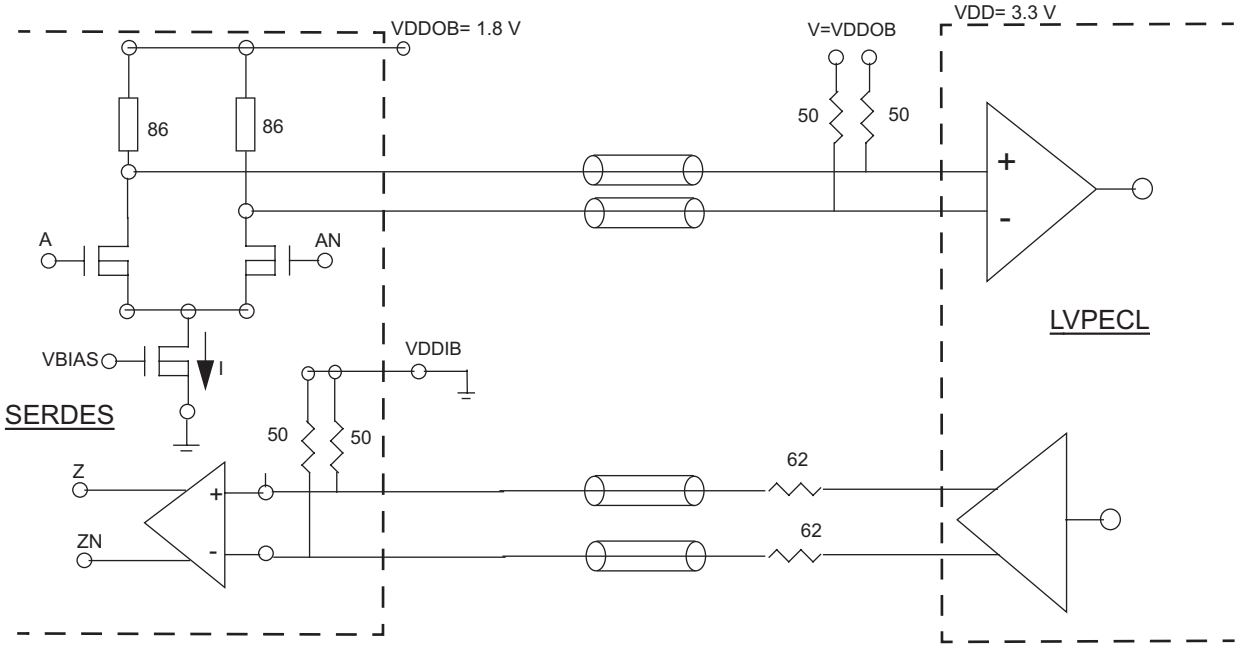
Table 5. Typical LVPECL I/O Specifications

Symbol	Parameter	Conditions	Min	Max	Units
Driver Specifications					
Voh	Output voltage high	Outputs terminated with 50 ohms to Vcc-2.0V	2215	2420	mV
Vol	Output voltage low	Outputs terminated with 50 ohms to Vcc-2.0V	1470	1680	mV
|Vod|	Output differential voltage	Outputs terminated with 50 ohms to Vcc-2.0V	535	950	mV
Ro	Output impedance, single ended	Vcm=1.0V to 1.4V	3	10	ohm
Receiver Specifications					
Vi	Input voltage range, common-mode	< 500mVp-p > 500mVp-p	1.1 1.3	3.1 3.1	V
|Vin-diff.|	Input voltage range, differential-mode		200	> 2000	mVp-p
Iih	Input HIGH current		-	150	uA
Iil	Input LOW current		-600	-	uA
Rin	Receiver differential input impedance	No internal termination resistor provided	>> 50	-	ohm

A comparison of Table 5 with Table 1 and Table 3 will show that significant signal I/O voltage and termination differences exist between LVPECL and SERDES. In both signal directions there is almost zero overlap in signal voltage range. To interface these technologies, signal voltage offset must be provided by the interconnection circuit.

The proposed circuit for SERDES to LVPECL interconnection is shown in Figure 7.

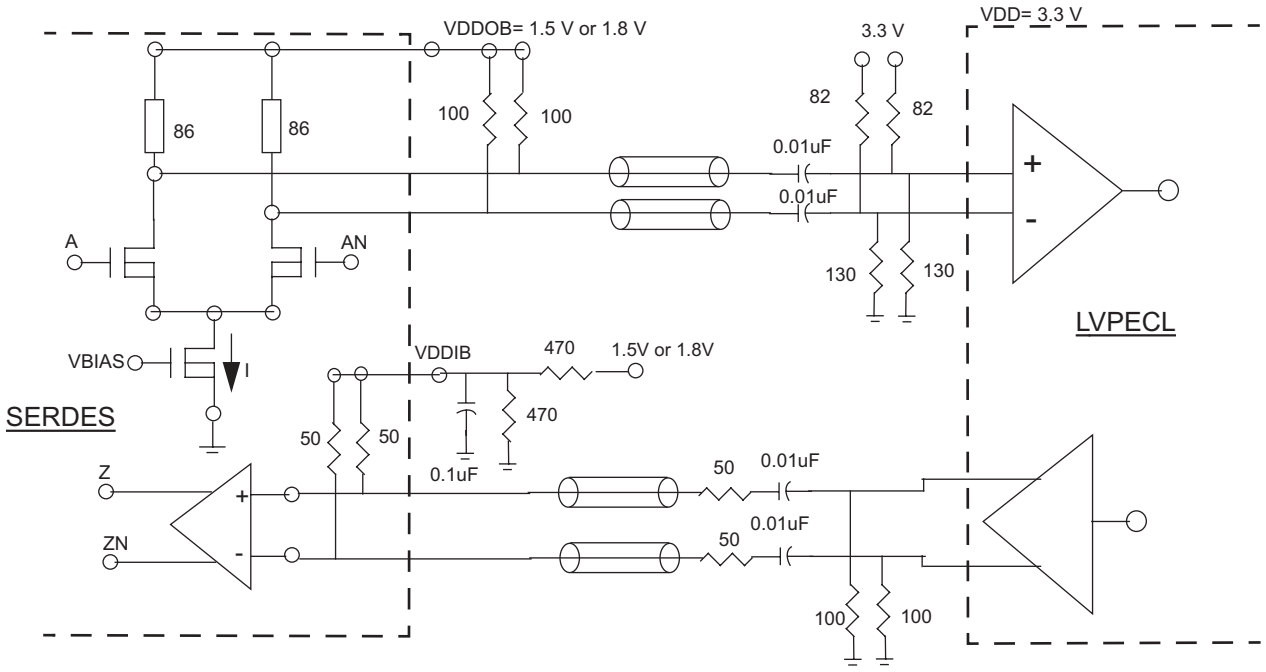
Figure 7. DC-Coupled LVPECL Interface



The circuit of Figure 7 minimizes external components and provides dc-signal coupling. The SERDES VDDOB supply is used at the LVPECL input to bias the two 50 ohm termination resistors, which characteristically terminate the transmission lines used for interconnection. The higher VDDOB value of 1.8V is preferred here to better align signal voltages. The LVPECL driver output bias current flows through the series 62 ohm resistors and the SERDES input internal 50 ohm termination resistors. This configuration provides the voltage offset and attenuation required for proper interface to the SERDES receiver. It also provides the matched transmission line termination for the interconnection.

Figure 8 shows an AC-coupled SERDES/ECL interface.

Figure 8. AC-Coupled LVPECL Interface.



This interface circuit requires a higher number of external components than the dc-coupled method, but will provide tolerance to higher levels of common-mode system and ground noise. This is achieved by biasing the signal common-mode voltage level near the center of the input range, at each receiver. This method offers flexible signal offset capability and can be adapted for use with 5V PECL and -5V ECL interface applications. For these cases, bias voltage and resistor value modifications are required.

Note that nominal resistor and capacitor values are shown in Figure 7 and Figure 8. Optimum values may vary in each application.

PCB, Connector and Cable Considerations

The sub-nanosecond rise time of the SERDES signals require very careful interconnection design techniques be used at the PCB level. The key to successful interconnection is using consistent transmission line paths with minimal discontinuities and true characteristic-impedance termination at the receive end of the line. Multi-layer laminated PCB backplanes and daughter cards are recommended, for best results. Use of controlled impedance connectors, PCB lines and cables provide the best result. Extensive test results for the ORT82G5 driving through a real backplane system, can be found in Reference 3. A good discussion of high-frequency PCB design considerations can be found in Reference 4.

Conclusion

Lattice SERDES serial I/O can be interfaced to LVDS, LVPECL, PECL and ECL technologies, as was described in this document. As with any high-speed electrical interface, success depends on very careful design at all levels, including the device package and printed wiring board design. Designers should follow good high-frequency PCB design practices, as described in Reference 4.

HSPICE models of the SERDES input and output buffers can be obtained through applications personnel. It is highly recommended that they be used to verify the performance of SERDES interface circuits, in all applications. High- frequency HSPICE models are available for many passive and active commercial components. Including these will increase the accuracy of the simulation results and provide higher confidence in the design integrity.

References

1. ORCA ORT82G5 and ORT42G5 Data Sheet
2. IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), IEEE Std 1596.3-1996
3. ORT82G5 FPSC High-speed Backplane Measurements, Lattice Technical Note 1027
4. ORCA ORSO82G5 and ORSO42G5 Data Sheet

SERDES Test Chip Jitter

Introduction

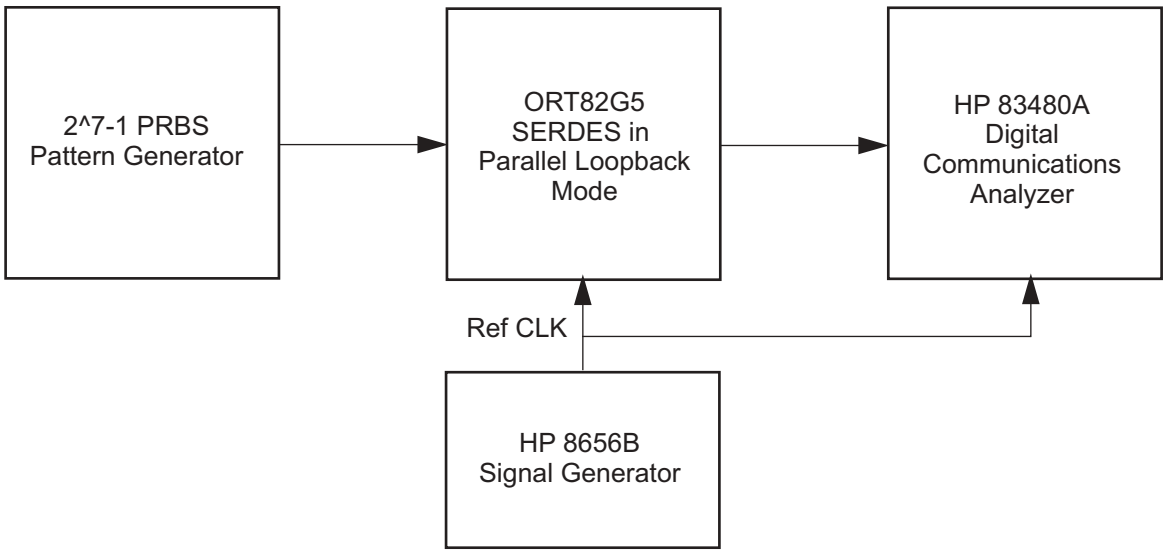
The ORT82G5 Field Programmable System Chip (FPSC)[1] contains two quad SERDES backplane interface blocks. The two quad SERDES provide eight high-speed serial channel interfaces that are capable of data rates up to 3.7 Gbits/s. Each channel can transmit and receive simultaneously and provides full clock and data recovery. At high data rates, jitter becomes a critical characteristic for error-free data transfer. This document discusses the device jitter performance and presents laboratory test results showing SERDES transmit and receive jitter characteristics. The test data was taken using a test chip that contained one quad macrocell, identical to the two quad macrocells on the ORT82G5.

Transmit Jitter

Total Jitter Measurement

The laboratory test setup used to measure total SERDES transmit jitter is shown in Figure 1.

Figure 1. Transmit (Total) Jitter Measurement Setup



The serial data rate for this test is 3.125 Gbits/s. A pseudo random bit stream test data pattern is applied to a SERDES channel, configured in parallel loop-back mode. The transmitter output waveform is observed in eye-diagram form with a HP83480A sampling digital communications analyzer. Peak-to-peak and RMS time-jitter at the 50 percent crossing level are calculated by the analyzer. The automated measurement process followed by the DCA includes digitizing waveform segments of the incoming data signal into 1350 data point sets, and acquiring 3000 of these waveform segments to calculate the jitter statistical parameters.

Test results are shown in Table 1. Three different devices with intentionally varied manufacturing process parameters, were used in this experiment. The designations Fast, Nominal and Slow are used in Table 1 to indicate the direction of each device bias. The purpose was to broaden device population that was represented in the experiment. Temperature and supply voltage variations were also included in the experiment.

Table 1. Transmit Jitter Measurement Result

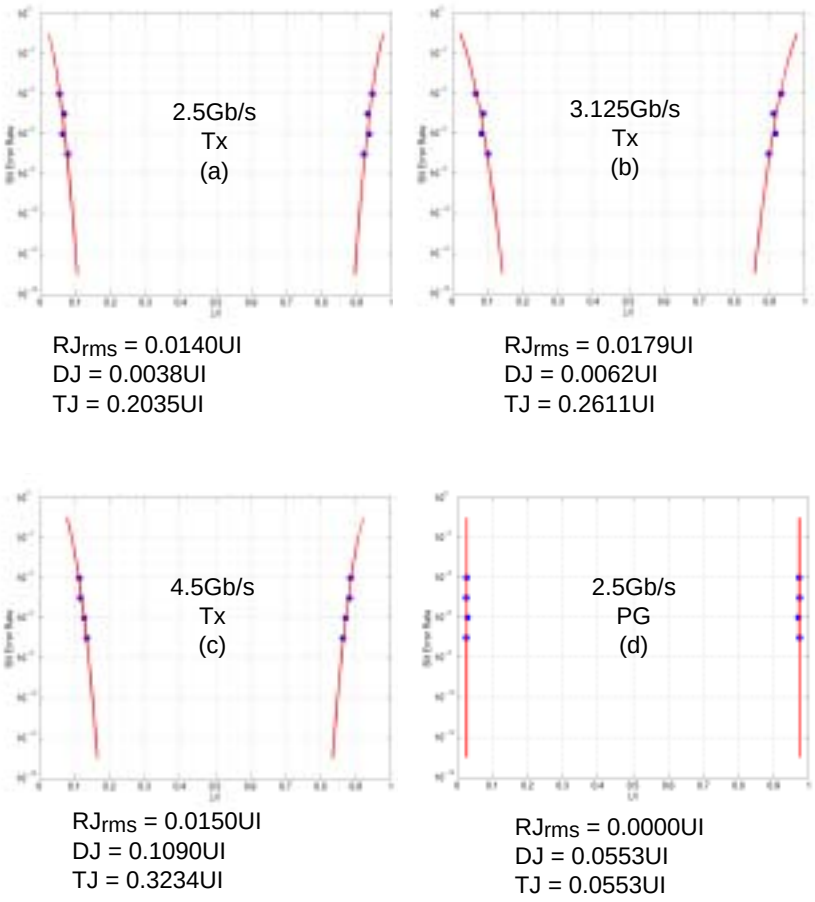
Device	Ambient Temperature	Voltage (V)	Tx Jitter pS RMS	Tx Jitter pS p-p	Tx Jitter (UI)
Nominal	0°C	1.5	6.0	40.0	0.125
Nominal	25°C	1.5	6.1	46.7	0.146
Nominal	85°C	1.5	6.2	44.4	0.139
Slow	0°C	1.5	6.5	46.7	0.146
Slow	25°C	1.5	6.6	44.4	0.139
Slow	85°C	1.5	7.2	48.9	0.153
Slow	85°C	1.575	7.2	51.1	0.160
Fast	0°C	1.5	5.7	42.2	0.132
Fast	25°C	1.5	6.8	46.7	0.146
Fast	85°C	1.5	7.9	55.6	0.174
Fast	0°C	1.575	5.5	42.2	0.132
Fast	0°C	1.425	8.3	53.3	0.167

The worst-case measurement seen in Table 1 shows a RMS jitter value of 8.3 pS and peak-to-peak value of 0.174 UI. All values in Table 1 are within the acceptable total jitter range for XAUI[3], Fibre Channel[4], and Infiniband[5] standards, although the test pattern used may not be the specific type specified in each standard.

Jitter Component Measurement

Emerging high-speed interface standards are requiring that the different jitter components be identified in measurements, and that each conform to specified limits. Appropriate measurement methods are still being devised and debated. One common measurement method for decomposing the total jitter (TJ) into a random component (RJ) and a deterministic component (DJ) is described in Reference 2. It uses a Bit-Error Rate Tester (BERT) combined with a Time Interval Analyzer (TIA) to generate transmit jitter bathtub-curve characterization. This is also discussed in Reference 2. Preliminary bathtub-curve testing of the ORT82G5 SERDES has been performed. Resulting bathtub-curves and the corresponding jitter component levels are shown in Figure 2. Curves measured at several different transmit data rates are shown, along with resulting jitter component breakdown for each curve.

Figure 2. Preliminary Bathtub-Curve Measurement Results



RJ_{rms} = 0.0140UI
DJ = 0.0038UI
TJ = 0.2035UI

RJ_{rms} = 0.0179UI
DJ = 0.0062UI
TJ = 0.2611UI

RJ_{rms} = 0.0150UI
DJ = 0.1090UI
TJ = 0.3234UI

RJ_{rms} = 0.0000UI
DJ = 0.0553UI
TJ = 0.0553UI

RJ = Random Jitter
DJ = Deterministic Jitter
TJ = Total Jitter

Receive Jitter Tolerance

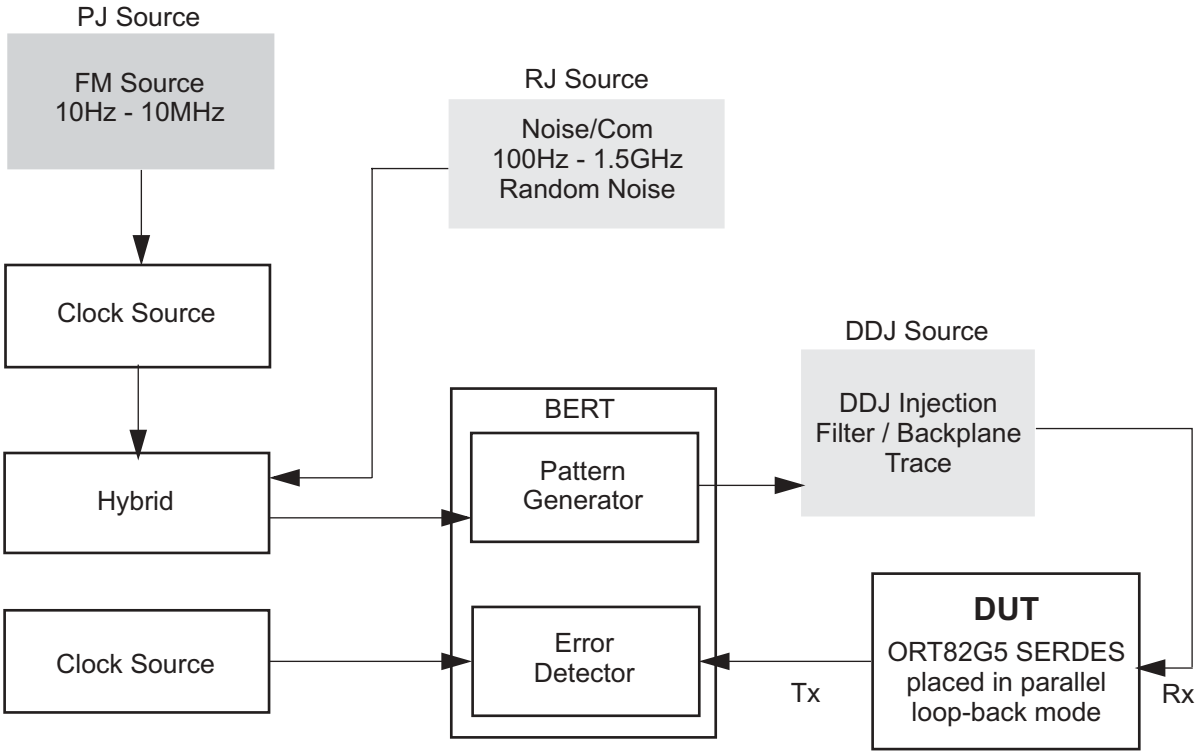
Receive jitter tolerance is a critical system interface parameter. It indicates the ability of the SERDES receiver to recover incoming serial data in the presence of transit signal jitter and path generated jitter that is generally additive. Such jitter will be present in all applications, in varying degrees, but must be kept within the limits of the receiver.

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High-speed serial interface standards have recognized this fact and have recently modified specifications to indicate tolerance levels for the different jitter types (such as those described in Section 2).

Jitter Tolerance Measurement

As with transmit jitter measurement methods, receive jitter tolerance measurement methods have not been firmly established. Preliminary test efforts have defined one test method which provides jitter components and levels as defined for the 10G Ethernet XAUI standard[3]. The test setup for this method is shown in Figure 3.

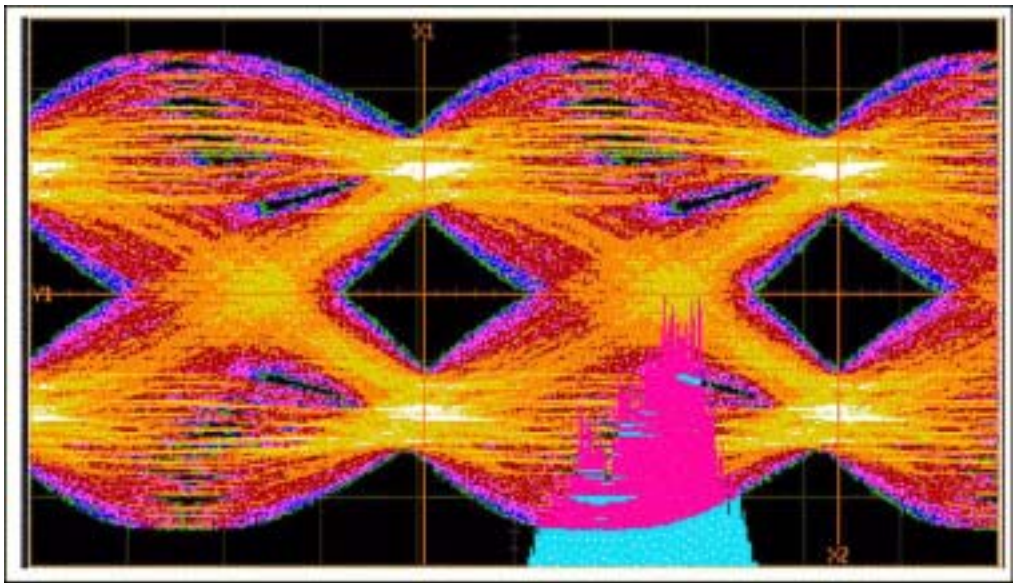
Figure 3. XAUI Receiver Jitter Tolerance Test Setup



PJ = sinusoidal periodic jitter
RJ = random jitter
DDJ = data dependent jitter

A detailed discussion of the test setup and procedure may be found in Reference 2. The measured eye-diagram of the incoming signal to the DUT in Figure 3, is shown in Figure 4.

Figure 4. Eye-Diagram for Receive Jitter Tolerance Test of Figure 3



Note that Figure 4 also shows a density function of the waveform level transition crossings through the center (horizontal) axis, between the second and third eye openings.

Jitter Tolerance Results

A pass/fail test was performed. Each jitter source component in the setup was adjusted to XAUI specified levels[3]. The same SERDES devices tested in Section 2 (and listed in Table 1) were used in this experiment. All temperature and supply voltage parameter levels, as specified in Table 1, were included in this testing. A CJT test data pattern was used. All testing performed passed the test criteria with measured bit error-rates of less than 1E-12.

Conclusion

Lattice FPSC SERDES transmit jitter generation and receive jitter tolerance have been measured and the results described. The results to date indicate excellent device performance in both of these areas. A summary of jitter requirements is shown in Table 2.

Table 2. Summary of Standards Jitter Requirements

Standard	Tx-Total Jitter	Rx-Jitter Tolerance
XAUI	0.35 UI	0.65 UI
Fibre Channel	0.65 UI*	0.70 UI*
Infiniband	0.35 UI	0.65 UI

*This standard is presently only specified at 1.065 Gbits/s rate

For the limited device test group used, all the transmit total-jitter measurement results were well within the limits of all three standards listed in Table 2. The XAUI receive jitter-tolerance tests showed standard limit compliance for the entire test group.

As system designers realize the importance of device jitter performance, standards and measurement methods are evolving and becoming more sophisticated. Additional device characterization is anticipated as the high-speed serial data interface standards mature.

References

1. Lattice ORT82G5 Field Programmable System Chip, Data Sheet

2. Jitter Testing for Multi-Gigabit Backplane SERDES, IEEE 2002 International Test Conference, Proceedings draft

3. IEEE Draft P802.3ae/D3.3, XGMII/XGMS/XAUI section, October 2001

4. FIBRE CHANNEL 10 Gigabit (10GFC), T11/Project 1413-D/Rev 1.1, May 11, 2001

5. InfiniBand Architecture Specification Volume 2, Release 1.0-a, June 19, 2001

Lock Times for the ORT82G5 and ORT42G5 SERDES

April 2003 Technical Note TN1025

Users of the ORT82G5 and ORT42G5 often are interested in the SERDES receiver's performance during acquisition and re-acquisition (locking) on to the incoming high-speed serial data stream. However, this term can have many meanings. For this reason, this note seeks to describe the various components of the acquisition process and report the results of measurements of each component.

The ORT82G5 and ORT42G5 SERDES RX logic performs four levels of synchronization on the incoming serial data stream. Each level builds upon the previous, providing first bit, then byte (character), then channel (32-bit word), and finally multichannel alignment. Each is described below.

Bit Alignment

Bit alignment is the task of the Clock/Data Recovery (CDR) block. This block utilizes a PLL that locks to the transitions in the incoming high-speed serial data stream, and outputs the extracted clock as well as the data. If the PLL is unable to lock to the serial data stream, it instead locks to REFCLK to stabilize the voltage-controlled oscillator (VCO), and periodically switches back to the serial data stream to again attempt synchronization. This process continues until a valid input data stream is detected and lock is achieved.

The CDR can maintain lock on data as long as the input data stream contains an adequate data "eye" (i.e., jitter is within specification), maximum data stream run length is not exceeded, and the average DC component of the signal is zero.

Bit alignment times fall into two categories: alignment from a no-signal condition, and re-alignment when the input serial data stream experiences an abrupt phase change (as may occur when protection switching is performed between two paths having different delays).

Alignment from a no-signal condition has two components. First, there is the re-acquisition to the data's frequency and phase. The time required for re-acquisition to the data's frequency is minimized by logic that periodically switches the PLL to lock to the REFCLK when it fails to lock on the serial data stream, thus limiting the VCO's frequency wander. Second, there is the time spent while the PLL is locking to REFCLK, which can be from zero to a nominal maximum value of approximately 30 microseconds, depending on when the serial data stream becomes valid in relation to the PLL's switching to/from REFCLK.

Re-alignment is very quick, since the PLL's VCO is already locked on frequency and only needs to adapt to the new phase. In the lab, this re-alignment has been observed to nominally require approximately 300 nanoseconds at 3.125 GHz, which is 938 bit times.

It is possible to avoid the 30-microsecond delay while the CDR re-aligns to the REFCLK by using Control Register bits ENBYSYNC‡ (to force synchronization to REFCLK) and/or TESTMODE‡ = E (to force synchronization to data). Using these signals, the CDR can be made to attempt to lock on data precisely when the data stream becomes valid. When these signals are used, care should be taken to ensure that the CDR's PLL frequency does not wander from its nominal value by limiting the time that the CDR is attempting to lock to an invalid data stream to 30 microseconds. If this time is exceeded, lock time will become excessive.

Byte Alignment

Byte alignment, as observed on signal BYTSYNC‡, occurs once valid bit alignment is achieved. The byte aligner looks for a particular 7-bit sequence (either 0011111 or its complement, 1100000) that, in data that has been 8B/10B encoded per IEEE 802.3, only occurs in the comma (/K/) characters K28.1, K28.5 and K28.7. Byte alignment only occurs when the ENBYSYNC‡ signal for that channel is active HI, and re-alignment occurs on each 7-bit sequence encountered. However, if ENBYSYNC‡ is asserted active HI and no comma character is encountered, and then is brought inactive LO, the channel will still perform one byte alignment operation on the next comma character.

Byte alignment occurs immediately when an alignment sequence is detected, so lock time is only one clock period.

Word (32-bit) Alignment

Word (32-bit) alignment requires that the Fibre-Channel (XAUI_MODE‡ = 0) or XAUI (XAUI_MODE‡ = 1) state machine has achieved the synchronized state.

Fibre-Channel Mode

In Fibre-Channel Mode, synchronization (WDSYNC‡ = 1) will occur after three ordered sets of data have been received, in the absence of any code violations. After this, the next comma character will cause the output data to be aligned such that the comma character is in the most significant byte. Thus, three ordered sets plus a comma character must be detected after byte sync is achieved before 32-bit word alignment occurs. The time required is directly dependent on comma-character density. This has been verified in the lab. Note: once word alignment is accomplished, no further alignment occurs unless and until WDSYNC goes to zero and back to one again. Comma characters that are not located in the most significant byte position will not trigger further re-alignment while WDSYNC is active. This behavior is as defined by the Fibre-Channel specification. But it means that, if the channel experiences an abrupt delay change (as could occur if an external MUX performs a protection switch between two links), and the delay change is close enough to a full character or characters that not enough code violations are generated to cause loss of WDSYNC, the channel could become misaligned and remain that way indefinitely. This behavior has been observed in the lab. As mentioned above, this is as defined by the Fibre-Channel specification. This behavior can be avoided by providing a set of three consecutive “idle ordered sets” so that correct alignment is guaranteed.

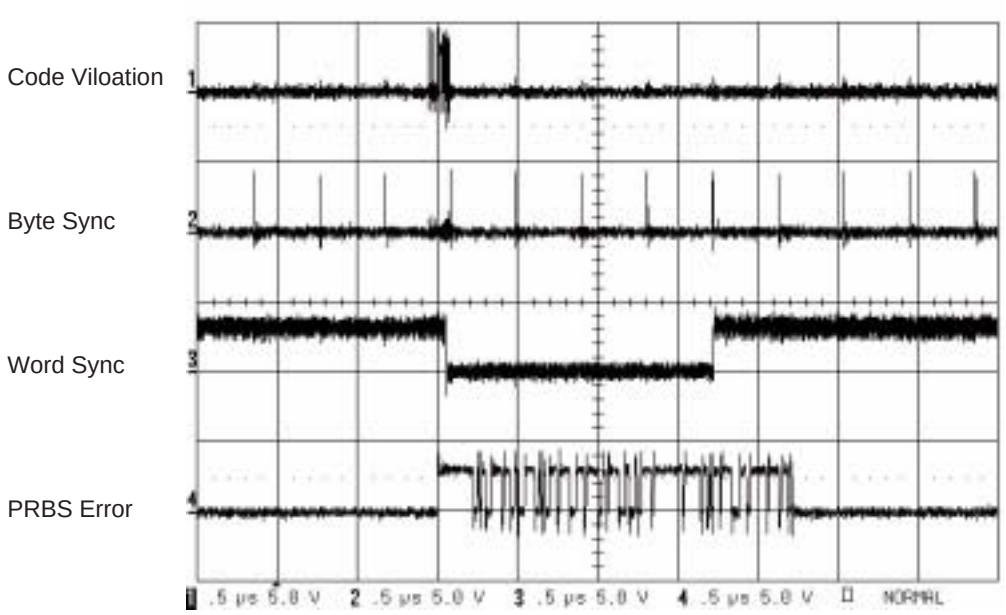
XAUI Mode

In XAUI mode, the state diagram in the data sheet indicates that three error-free code-groups containing commas must be detected before synchronization is declared.

Multi (2, 4 or 8) Channel Alignment

Multi (2, 4 or 8) channel alignment does not occur until after 32-bit word alignment is complete. Alignment will not occur until the last (most delayed) channel has been received. The maximum skew between the earliest and latest channels cannot be greater than 18 cycles of the parallel receive data clock RWCK. At 78.125 MHz, this is 12.8 ns X 18 = 230.4 ns maximum.

Figure 1. Re-Lock After Positive Loop Delay Change



Re-Lock After Abrupt Loop Delay Change

Figure 1 displays the performance of the ORT82G5 and ORT42G5 when the high-speed serial bit stream experiences an abrupt loop delay change in the serial link. Here, the delay change is caused by a switch into or out of internal loopback, where the non-loopback path is looped back externally. The transmitter is sending an idle ordered set every 32nd word. Code violations mark the beginning of the abrupt delay change. When the receiver re-establishes phase lock and a comma character is recognized, code violations cease. Three comma characters later, word sync is re-established. Word alignment is performed on the next comma character, at which time the PRBS data checker implemented in the FPGA ceases to report errors.

Conclusion

In conclusion, the “lock time” can mean many things, but breaks down into the components outlined above: bit, byte, word and multi-channel alignment. Once the chip has recovered from reset and REFCLK is stable, the time required to lock onto a high-speed serial data stream is sub-microsecond. Further time required for byte synchronization, word synchronization, word alignment and multi-channel alignment depends on density of comma characters: one for byte sync, three for word sync, and one for word alignment. Multi-channel alignment occurs shortly after the latest channel arrives. Table 1 below summarizes these values.

Table 1. Summary of Lock Times

Synchronization Type	Lock Time
Initial Bit Alignment	1-31 µsec
Bit Realignment	300 nsec (938 bit times @ 3.125 GHz) nominal
Byte Alignment	Immediately upon encountering first comma character
Word Alignment	After encountering 3 additional comma characters (see text for further Fibre-Channel and XAUI mode details)
Multi-Channel Alignment	After alignment characters received from all channels being aligned

‡ Note: The various reference points mentioned in this article can be accessed as listed in Table 2 below.

Table 2. List of Access Points

	AA	AB	AC	AD	BA	BB	BC	BD
XAUI_MODE	30820 (7)				30920 (7)			
Testmode (4:0)	30006 (4:0)	30016 (4:0)	30026 (4:0)	30036 (4:0)	30106 (4:0)	30116 (4:0)	30126 (4:0)	30136 (4:0)
ENBYSYNC	30800 (0)	30800 (1)	30800 (2)	30800 (3)	30900 (0)	30900 (1)	30900 (2)	30900 (3)
BYTSYNC	Not observable				Observable, one channel at a time, on characterization port pin AH31			
WDSYNC	Not observable				Observable, one channel at a time, on characterization port pin AJ34			

SERDES Reference Clock

April 2003 Technical Note TN1040

Introduction

This document discusses the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 FPSC devices [1] reference clock input characteristics and the selection/interconnection of the external reference clock source. The reference clock signal quality is critical to SERDES high speed signal interfaces, as is demonstrated in Appendix A. Clock signal jitter can cause jitter generation at the transmit data output port and affect jitter tolerance of receiver data input port. Care must be taken in the selection and connection of the reference clock source to obtain optimum jitter performance. Several possible commercial oscillator manufacturers are identified and alternative interconnections circuits are presented.

Reference Clock Input Characteristics

The ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 provide two separate REFCLK differential inputs, to allow device operation under two different clock domains. Each REFCLK input port services four of the eight available SERDES channels. Each differential input port has an internal differential amplifier with significant common-mode signal rejection characteristics. The minimum required differential input level requirement is 500 mVp-p. The maximum input is 2 Vp-p. The input common-mode voltage may be set to any level which maintains each input peak voltage between VDD and ground potential.

Clock Source Selection

A crystal oscillator or crystal oscillator-based clock source with differential output is recommended. The experiment described in Appendix A shows that reference clock signal jitter does contribute directly to SERDES transmit signal jitter. It is therefore important to select a clock source with low jitter characteristics.The source should contain power supply decoupling (internal and/or external) and ideally be located on the same circuit board as the SERDES device.

A number of crystal oscillator products on the market are compatible with the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5. Several are listed in the table below.

Table 1. Crystal Oscillator Products Compatible with the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 Devices

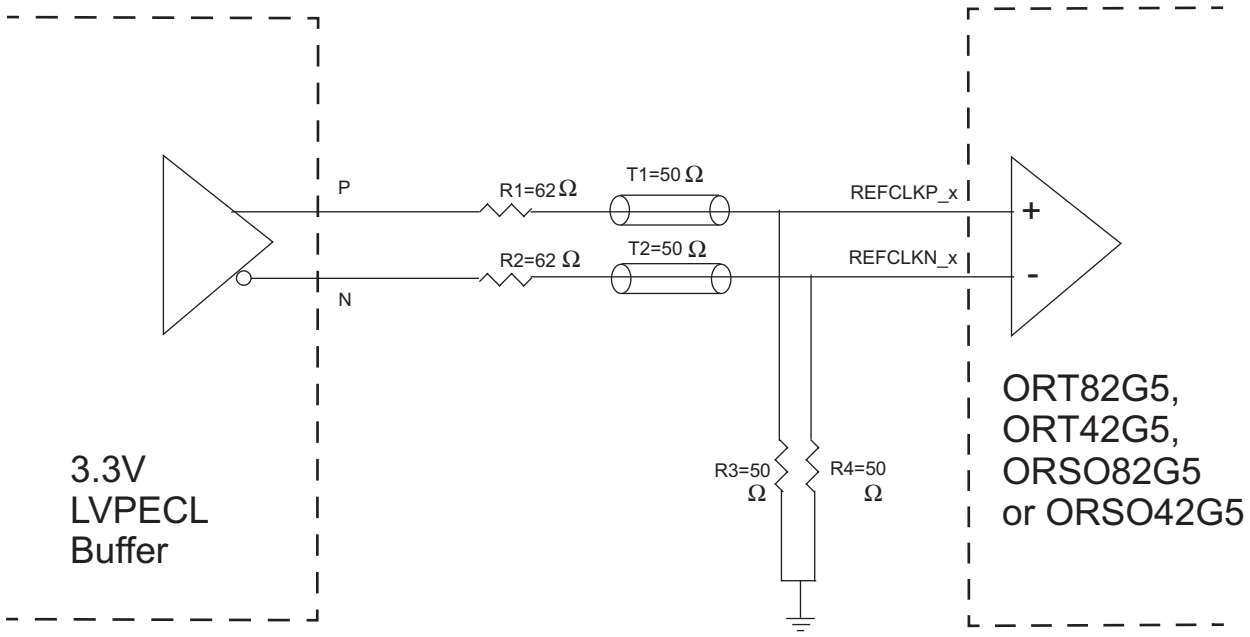
Vendor	Model	Output	Comments
Connor Winfield [6]	P123	LVPECL	small size SMD package
Epson [3]	EG-2101CA	PECL	SMD package, 50ppm
MF Electronics [5]	M2980	LVPECL	thru-hole/ gull-wing pkg, low jitter specified
Saronix [2]	SDS3811	LVDS	SMD package, to 20ppm
Vectron [4]	XO-480	LVPECL or LVDS	SMD package, to 10ppm

Interconnection Circuit Alternatives

A differential output interconnection to the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 is recommended to minimize the conversion of system common mode noise into clock signal jitter. This is achieved by taking advantage of the common-mode rejection of the internal differential receiver. If the source signal is shared with other devices or inputs on the circuit board, it is recommended that high speed differential buffering be provided to distribute a dedicated differential output signal to each device reference clock input.

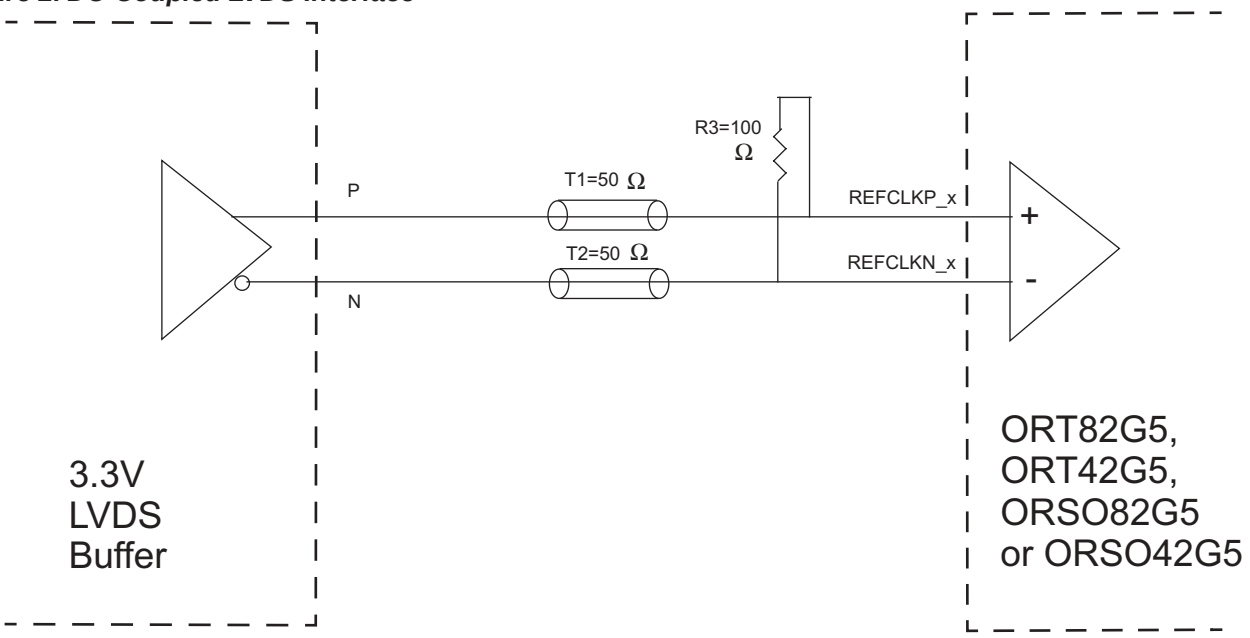
The recommended interconnection of a 3.3V LVPECL Reference Clock source to the Quad SERDES input port is shown in Figure 1.

Figure 1. DC Coupled LVPECL Interface



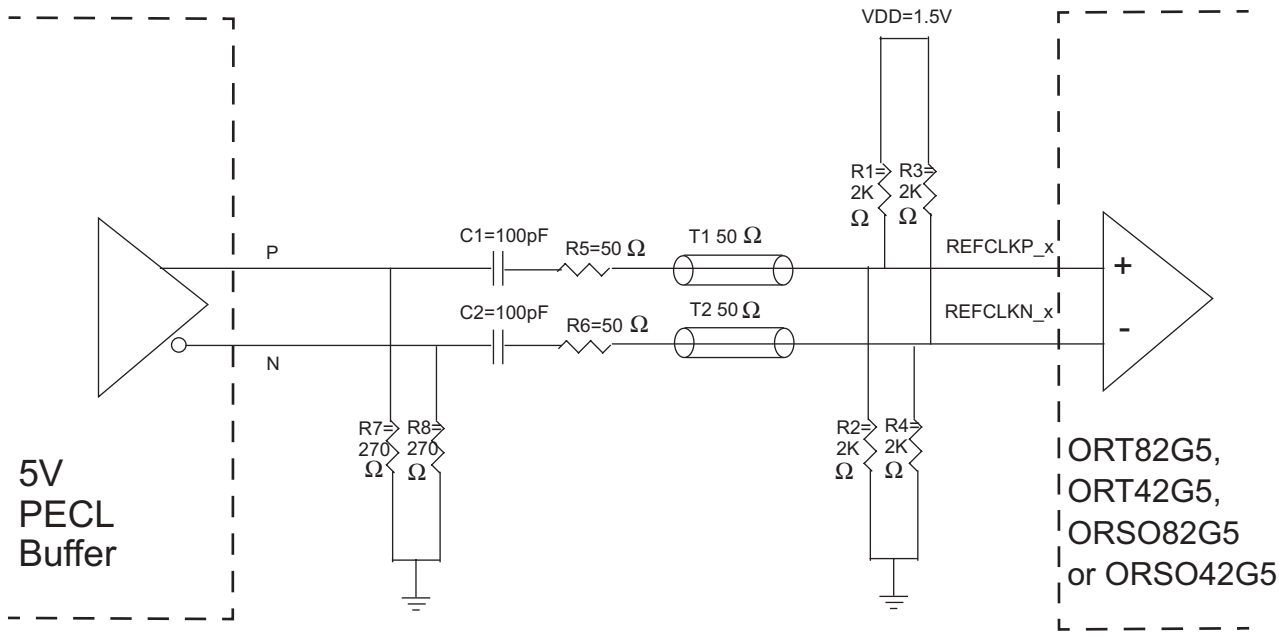
The dc coupling scheme from the 3.3V LVPECL clock signal buffer output allows a minimal number of discrete components in the interconnection circuit.

Figure 2. DC-Coupled LVDS Interface



The standard LVDS output dc voltage is compatible with the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 RefClk input, allowing a very simple interface circuit. The single termination resistor should minimize the possibility of system generated EM noise coupling into the reference clock signal.

Figure 3. AC-Coupled PECL Interface



A conventional ECL source terminated configuration is used with ac coupling. Resistive voltage divider biasing of the Reference Clock input pins must be provided.

Applications where SERDES jitter performance is not critical may consider using single-ended reference clock interconnections. Such interconnections have been successfully used in laboratory testing. For these cases, external biasing and capacitive bypassing of the unused input must be provided. These applications may also choose to drive both reference clock ports of the ORT82G5, ORT42G5, ORSO82G5 or ORSO42G5 with a single clock source output. Care must be taken to minimize trace lengths between the transmission line, line termination resistors, and Reference Clock input pins.

PCB Layout Recommendations

To minimize differential clock signal noise and jitter at the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 device input, the T1/T2 transmission line connection path should have the following characteristics:

- adjacent stripline point-to-point 50 ohm transmission lines or coupled adjacent lines with 100 ohm differential characteristic impedance
- matched length, to within 0.05 inch (1.27mm)
- cross-talk coupling to other signal traces on the PCB minimized
- stripline implementation
- The discrete components in Figures 1 and 3 should be placed according to the following recommendations:
- PCB connection trace lengths should be kept as short as possible.
- Corresponding components on the P and N signal sides should be placed close to each other, to minimize system coupled differential noise.

Conclusion

The ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 SERDES jitter performance is sensitive to the external reference clock signal jitter. For best performance, a differential transmission line clock signal should be used. Interconnection circuits for several oscillator output formats were recommended and described. Careful PCB layout with some specific recommendations was presented. Several possible oscillator vendors were identified.

References

1. ORCA ORT82G5 and ORT42G5 Data Sheet
2. Saronix, http://www.saronix.com/
3. Epson Electronics America, http://www.eea.epson.com/go/products/displayCategory?categoryId=EEA.QD.Crystal_Oscillators
4. Vectron International, http://www.vectron.com/
5. MF Electronics, http://www.mfelectronics.com/products/xo/
6. Connor Winfield, http://www.conwin.com
7. ORCA ORSO82G5 and ORSO42G5 Data Sheet

Appendix A - SERDES Jitter Sensitivity

A simple experiment was performed in the laboratory to determine the effect of reference clock input jitter on ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 SERDES transmit jitter. Sinusoidal jitter was injected onto the reference clock signal, while observing SERDES output signal jitter. DCA measured eye-diagram waveforms of the data output signal and reference clock input signal are shown in the following 4 figures. Figure 4 is with no jitter added. Figures 5, 6, and 7 are with sinusoidal jitter added to the reference clock signal. The frequency of the jitter signal is indicated in each of these figures. Note that in all four Figures, a density function of the reference clock transitions (horizontal axis crossing, at the center level) is shown.

Figure 4. Transmit Data Output & Ref Clk Eye-Diagrams with No Jitter Added

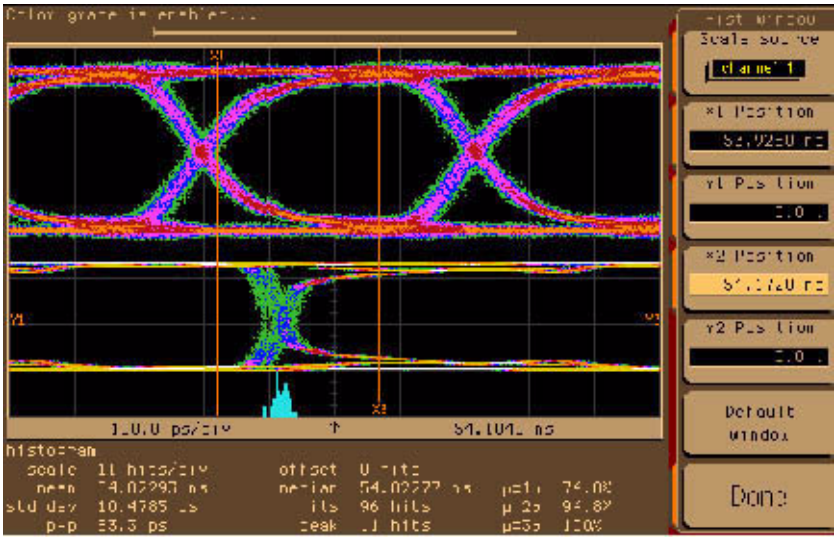


Figure 5. Transmit Data Output & Ref Clk Eye-Diagrams with 10 KHz Jitter Added

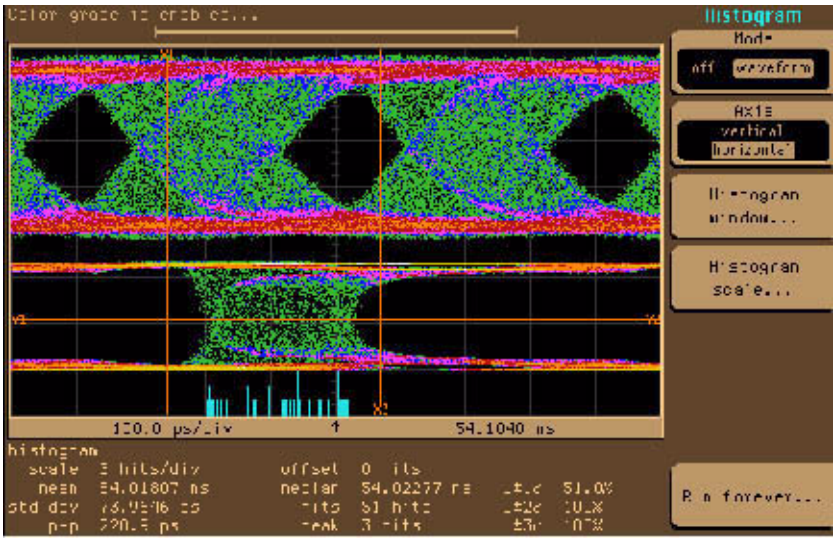


Figure 6. Transmit Data Output & Ref Clk Eye-Diagrams with 100 KHz Jitter Added

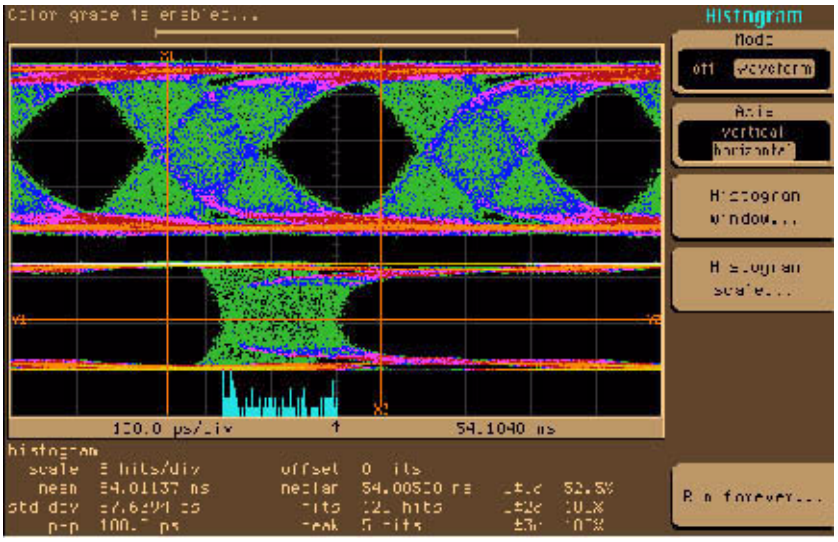
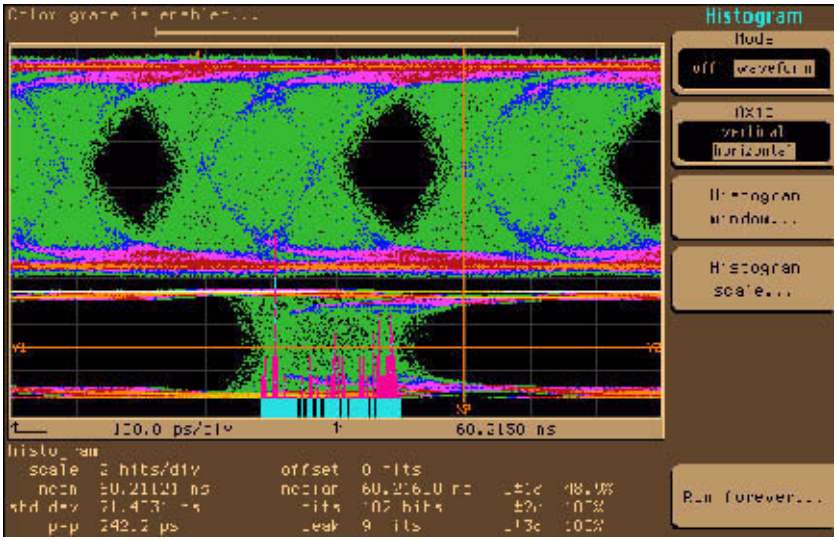


Figure 7. Transmit Data Output & Ref Clk Eye-Diagrams with 500 KHz Jitter Added



Discussion

Comparing Figure 4 to Figure 5, it can been seen that adding jitter to the reference clock signal causes an increase in transmitter output signal jitter. Observing the amount of jitter on the two waveforms in Figures 5 through Figure 7, it can be seen they are approximately the same. The conclusion drawn from this experiment is that there is a 1 to 1 jitter transfer from the reference clock signal to the transmit output signal. This is an expected result which will apply to jitter frequencies below about 5 MHz (the closed loop bandwidth of the SERDES transmit clock PLL).

Introduction to the sysHSI™ Block ispXPGA™ and ispGDX2™

April 2003 Technical Note

Introduction

Embedding clocks into serial data streams is a popular technique in high-speed data communications systems applications. The embedded clock is recovered at the receiver by a Clock and Data Recovery (CDR) circuit. Source Synchronous mode provides another way of achieving high speed data rate without embedding the clock.

Lattice provides sysHSI blocks on ispXPGA and ispGDX2 device families to support both embedded clock and source synchronous clocking applications. This document provides an introduction to the sysHSI Blocks. Refer to Technical Note TN1020 for detailed description.

Modes of Operation

The sysHSI block supports number of different modes. In Clock Data Recovery (CDR) mode, clock is encoded in the transmit data stream and CDR recovers this clock from the incoming data. In Source Synchronous Mode, clock is transmitted along with data via a separate channel.

Three fuse programmable modes and their related system specifications are summarized in Table 1.

Table 1. Fuse Programmable Modes

Mode	Data Code	Serial Data Rate (Mbps)	Pay Load Data Rate (Mbps)	Parallel Data/Clk (MHz)	Parallel Data Width	Serial/ Parallel Ratio	Symbol Alignment Pattern	CDR Support
SERDES without Encoding/Decoding	8B/10B	400 to 850	320 to 680	40 to 85	10b Encoded	10	K28.5 +/-	CDR
SERDES with Encoding/Decoding	10B/12B	400 to 850	333 to 708	33.3 to 70.8	10b Raw Data	12	SymPat	CDR
Source-Synchronous (n channels)	N/A	400 to 800	n x (400 to 800)	50 to 100 67 to 133 100 to 200	n x 8b n x 6b n x 4b	8 6 4	SymPat[1] (De-skew)	De-skew (optional)

1. In Source-Synchronous mode, only De-skew mode requires symbol alignment.

CDR Mode

In CDR mode clock is encoded in serial data streams to achieve higher data transfer rates. This is achieved by encoding the transmitted data in such a way as to ensure a minimum number of clock transitions. From this minimum number of transitions a complete clock can be recovered at the receiver.

The sysHSI block supports two encoding options. In both options the sysHSI block recovers data using 16 times over-sampling. This leads to better performance than many other solutions that use lower over-sampling rates.

SERDES without Encoding/Decoding (8B/10B: Encoding and Decoding is not included)
This mode supports serial links that use the common 8B/10B encoding scheme. With this scheme eight bits of data are encoded into 10 bit symbols to ensure a minimum of 40% transition in every 10-bit code.

In 8B/10B mode the sysHSI block does not encode or decode the data. The block receives encoded 8B/10B data as 10-bit wide parallel data and transmits it serially. It receives serial data and converts it to 10-bit wide 8B/10B encoded data. This data can be re-transmitted or decoded elsewhere dependent on the application needs.

SERDES with Encoding (10B/12B: Encoding and Decoding is done by sysHSI Block)
This mode supports serial links that use 10B/12B encoding. This high speed serial data format consists of 10 data bits plus 2 fixed insertion bits (01) to ensure a minimum of two transitions for every 12 bits in the serial data stream.

Source-Synchronous(SS) Modes

Some users are implementing source synchronous clocking to achieve high speed data transfer. Here the clock is transmitted along with the data. This removes the propagation delay between the transmitter and receiver as a limit on clock speed and performance. Skew control and other factors limit the maximum performance that can be achieved using this method of data transfer. Multiple sysHSI blocks can be combined to create source synchronous interfaces of different widths. The maximum width supported is device dependent. These interfaces can operate in two modes.

Normal Mode SS Mode (with Optional Phase Adjustment)
Normal Mode without Phase Adjustment:
In normal source synchronous mode data for each channel is captured using a common phase shifted version of the incoming clock. This mode is useful in smaller devices where clock-tree skew is minimum.

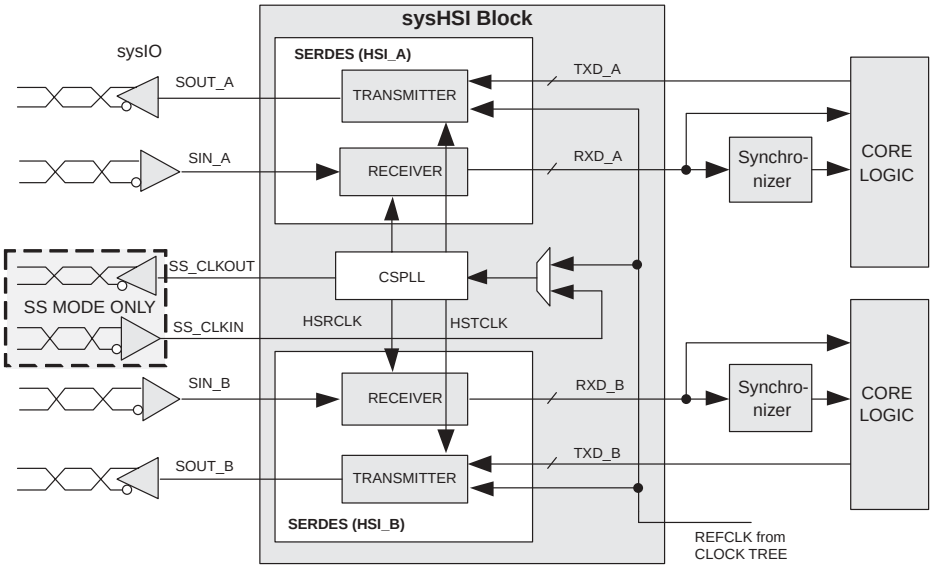
Normal Mode with Phase Adjustment:
Optional Phase Adjustment is provided in this mode. The known skew adjustment phase value can be programmed by user.

De-Skew SS Mode
In this mode, a calibration cycle allows the CDR circuitry to be used to select per channel different phases of the incoming clock with which to capture the incoming data. This allows the device to compensate for fixed system level skews. Thus allowing designers to achieve higher performance by conducting a calibration cycle at system start up.

sysHSI Block

Each sysHSI Block includes two SERDES units and one CSPLL. Each SERDES unit consists of one receiver and one transmitter circuit block. Each pair of receiver and transmitter can be used as a full duplex channel. For receiving, the SERDES receives high speed serial input data stream from the sysIO differential input buffer and provides low speed parallel data associated with recovered clock to synchronizer or core logic. For transmitting, the SERDES converts the parallel low speed data to high speed serial data stream and sends the data to the sysIO LVDS differential output buffers. Figure 1 shows high level representation of a sysHSI Block.

Figure 1. sysHSI Block Diagram



There is always a 10-bit wide data transmitted or received at the low speed side of the SERDES for both 10B/12B and 8B/10B modes. In 10B/12B encoding mode, the start bit(1) and stop bit(0) are added or removed within the sysHSI Block. In SERDES mode without encoding/decoding, (currently 8B/10B mode is supported), the encoding

and decoding is done outside of sysHSI Block where 10-bit wide data is expected at the low speed side of the SERDES. This is why the number of data bits at the parallel interface for 10B/12B and 8B/10B are same. In Source Synchronous Mode, the low speed parallel data bits can be programmed to 4, 6 or 8.

The recovered clock is asynchronous to the on-chip reference clock. The solution to this problem is to use a synchronizer. In systems where frequency deviation is not a problem this synchronizer can be bypassed.

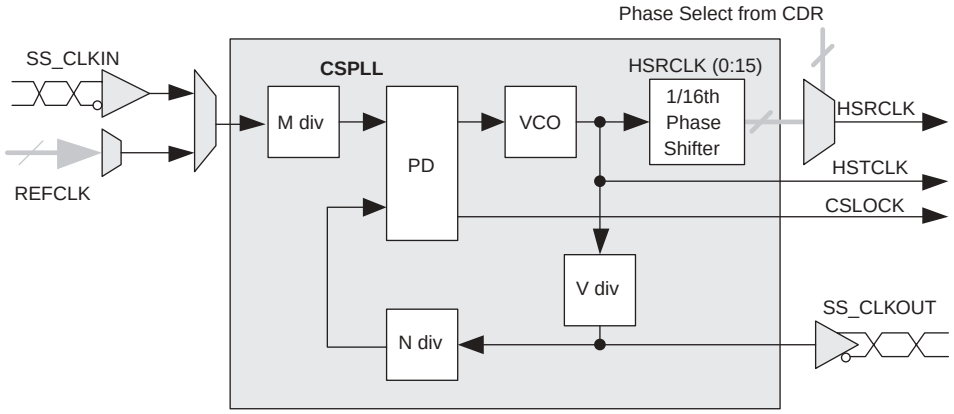
CSPLL: Clock Synthesizer PLL

CSPLL (Clock Synthesizer PLL) multiplies low speed reference clock by the factor of v to achieve an high speed serial data rate clock. The low speed reference clock input can be either from a chip internal clock, REFCLK, or from an external LVDS clock input, SS_CLKIN. Also, there are 4 choices for the internal clock to increase the flexibility.

\The multiplication factor, v, is the ratio of high speed vs. low speed. It can be 4, 6, or 8 for Source Synchronous mode, 12 for 10B/12B and 10 for 8B/10B mode. CSPLL contains a fully monolithic analog PLL which does not require any external component. For transmitter, the HSTCLK (High Speed Transmit Clock) is generated from REFCLK multiplied by factor of 'v', and is used to clock the high speed Serial Data Output.

For CDR operation, the CSPLL combined with a phase interpolation circuit, generate 16- phase high speed Clocks, HSRCLK<0:15>(High Speed Receive Clock).

Figure 2. CSPLL

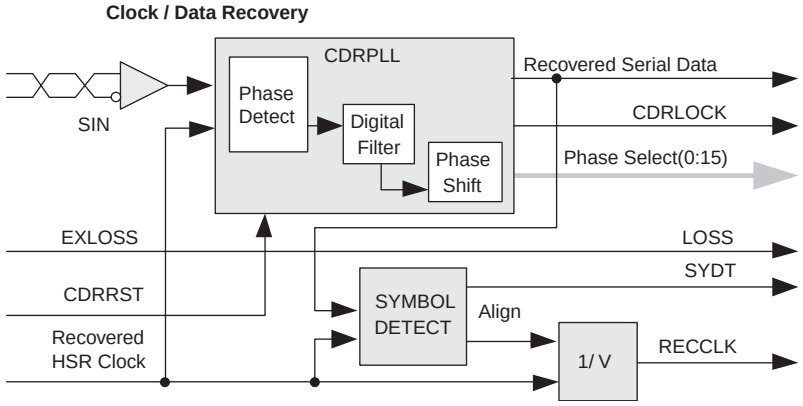


Clock and Data Recovery

Each receiver channel has its own CDRPLL (Digital Phase-Locked Loop: DPLL) for Clock Data Recovery. The Clock Recovery module first extracts the embedded high speed clock from the Input Serial Data Stream by means of the CDRPLL. Then the Data Recovery Module uses the recovered clock to read the data from the high speed Input Serial Data Stream.

The recovered high speed clock is divided by the factor, v, and aligned to produce the low speed clock, RECCLK (RECovered CLocK). CDR then de-serializes the recovered high speed Serial Data into low speed Parallel Data. This RECCLK and parallel data are sent to synchronizer or core logic.

Figure 3. Clock and Data Recovery Block

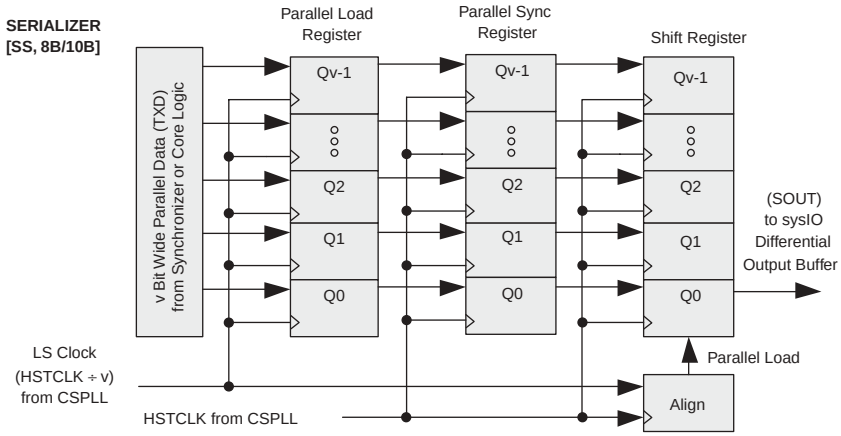


Serializer / De-Serializer(SER/DES)

Serializer

Transmitter receives low speed parallel Data, TXD, from the Synchronizer or Core Logic. TXD data is clocked by REFCLK from clock tree (or SS_CLKIN in SS mode). The CSPLL multiplies REFCLK by factor of v to generate HSTCLK. The Transmitter converts the low speed parallel Data, TXD, into high speed Serial Data Stream, SOUT, that is running at HSTCLK. The alignment circuit synchronizes REFCLK and HSTCLK with edge detect circuit to align SOUT with HSTCLK.

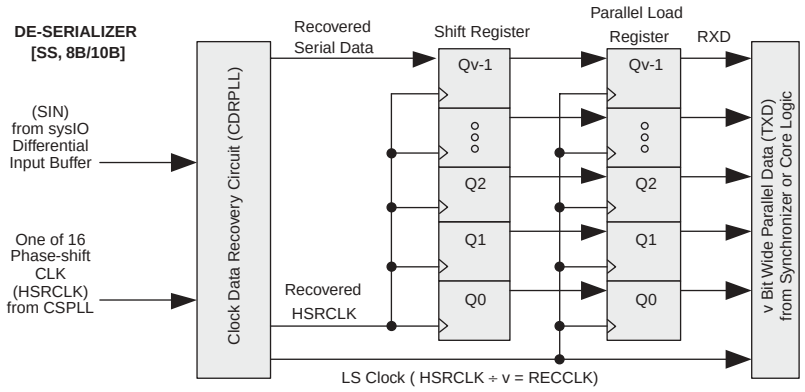
Figure 4. Serializer [SS, 8B/10B]



De-Serializer

Receiver receives high speed serial data stream, SIN, from sysIO and de-serializes into low speed Parallel Data, RXD, before it sends to Synchronizer or core logic.

Figure 5. De-Serializer [SS, 8B/10B]

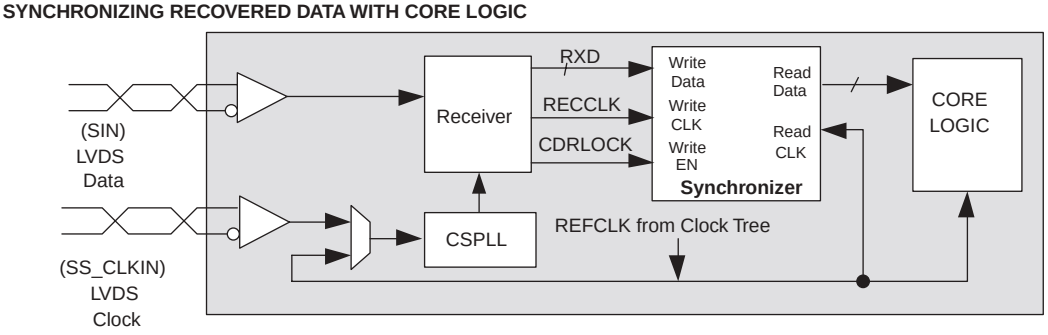


Synchronizer

In the Receiver, the sysHSI Block writes with Recovered Clock (RECCLK) and the Core Logic uses system clock (usually REFCLK) to read. Depending on devices, FIFO or Embedded Memory Block are used as a synchronizer. The usage of a synchronizer is optional and may be bypassed if users performs synchronization outside of the device.

Parallel Transmit Data enters Transmitter of sysHSI block from core logic clocked by REFCLK. The REFCLK at the same time is fed to CSPLL to generate high speed clock to transmit serialized data (HSTCLK). In the Transmitter, the REFCLK is re-aligned by high speed clock to generate parallel load clock to the Serializer shift register. If the skew between REFCLK and high speed Clock at Transmitter is larger than one high speed Clock cycle then a synchronizer is required. Since the CSPLL drives only two transmitter and two receiver channels, the skew is manageable without synchronizer. Figure 6 shows the synchronizer interface between core logic and receiver.

Figure 6. Synchronizer



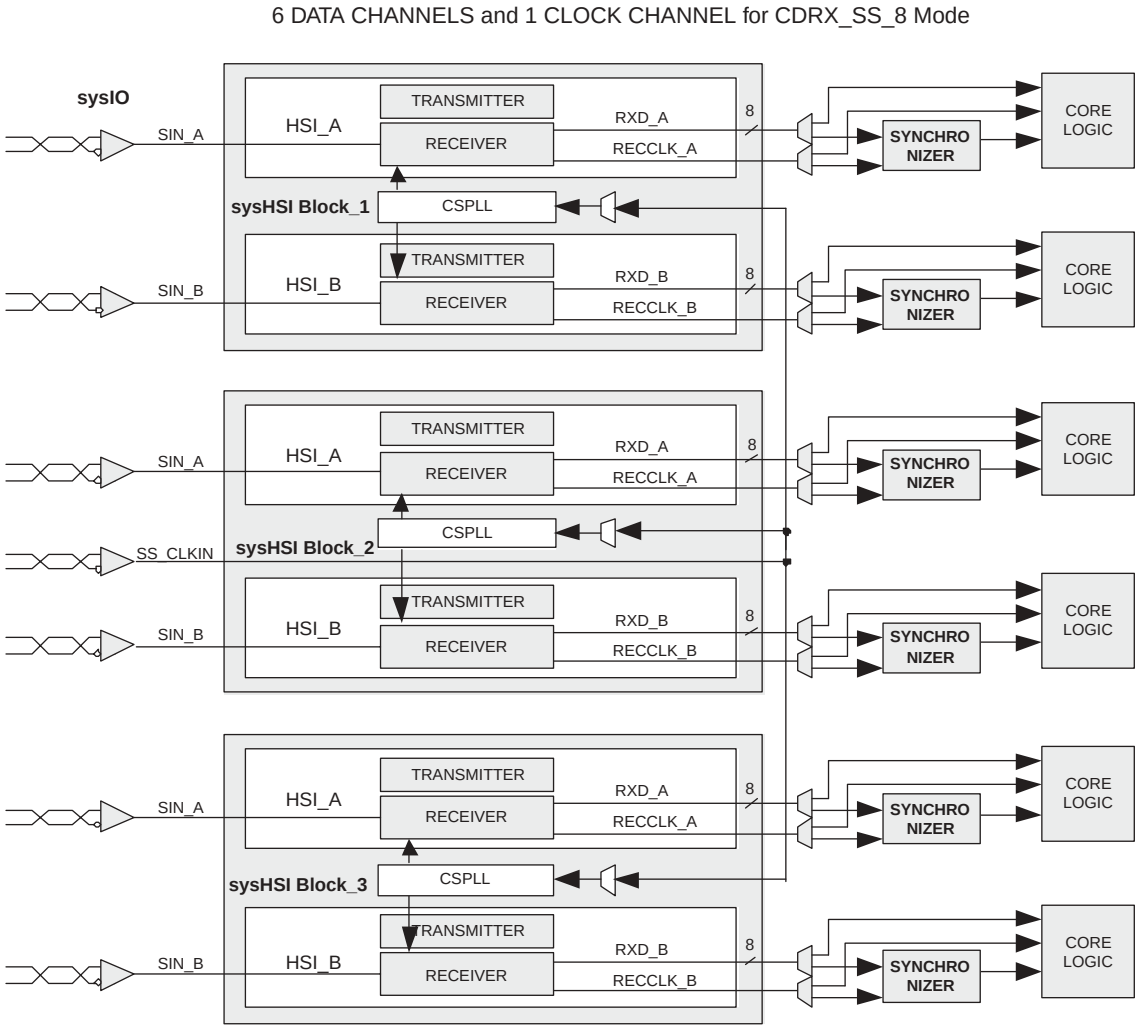
sysHSI Block and Source-Synchronous Mode with Multiple Data Channels

Each chip includes 2 groups of sysHSI Blocks. All sysHSI Blocks of the same group share the same LVDS clock input/output in Source Synchronous mode.

In this mode, a whole group or a portion of a group can be used. The LVDS Clocks, SS_CLKIN and SS_CLKOUT, are connected to dedicated pins. Each group can be configured as either Receive mode or Transmit mode but not both. In Receive mode, the incoming LVDS Clock (SS_CLKIN) is the input clock to CSPLL as a reference clock . In Transmit mode, the reference clock source is one of four clocks from the Clock Tree. The LVDS output Clock, SS_CLKOUT is generated from the CSPLL of the dedicated sysHSI Block in each group.

An example of Source-Synchronous Mode Block diagram is shown in Figure 7. Figure 7 illustrates how the HSI circuit is implemented in Source-Synchronous Receiver Mode.

Figure 7. Source-Synchronous Mode Example Diagram (CDRX_SS_8)



sysHSI Block Usage in CDR Mode

When both channels are used in a same sysHSI Block, they must share the same REFCLK, HSRCLK (High Speed Receiver Clock) and HSTCLK (High Speed Transmitter Clock) from the CSPLL. Multiple modes may be implemented using different sysHSI Blocks but user must take phase jitter from different clock sources into consideration. This jitter increase may both receiver and transmitter performance to fall outside the guaranteed specifications.

The two SERDES Blocks, HSI_A and HSI_B, in the same sysHSI Block are independent from each other except sharing the same REFCLK and CSPLL.

sysHSI Block USAGE in Source-Synchronous Mode

When sysHSI Blocks are configured as Source-Synchronous mode, the whole group is not available for other modes. But the sysIOs of unused sysHSI channels are available for other general I/O uses.

Using sysHSI Blocks in Design Tools

Macro Symbols

Thirteen Functional Macro modules are available representing seven different applications. These programmable modules are described in Table 2. Additionally, two macros are provided for high speed loop back testing and are supported for 8B/10B and 10B/12B modes.

Table 2. Macro Definitions

Mode	Symbol	Description
SS	RX_SS_x[1]	SS normal receive mode (no de-skew)
	CDRX_ SS_x	SS De-skew receive mode
	TX_ SS_x	SS transmit mode
10B12B	CDRX_10B12B	10B/12B CDR receive mode
	TX_10B12B	10B/12B transmit mode
8B10B	CDRX_8B10B	8B/10B CDR receive mode
	TX_8B10B	8B/10B transmit mode
8B10B	HSLB_8B10B	8B/10B High Speed Loop Back mode
10B12B	HSLB_10B12B	10B/12B High Speed Loop Back mode

1. x: Data width, 4, 6 or 8 resulting the total number of macros are 15.

sysHSI Usage with HDLs

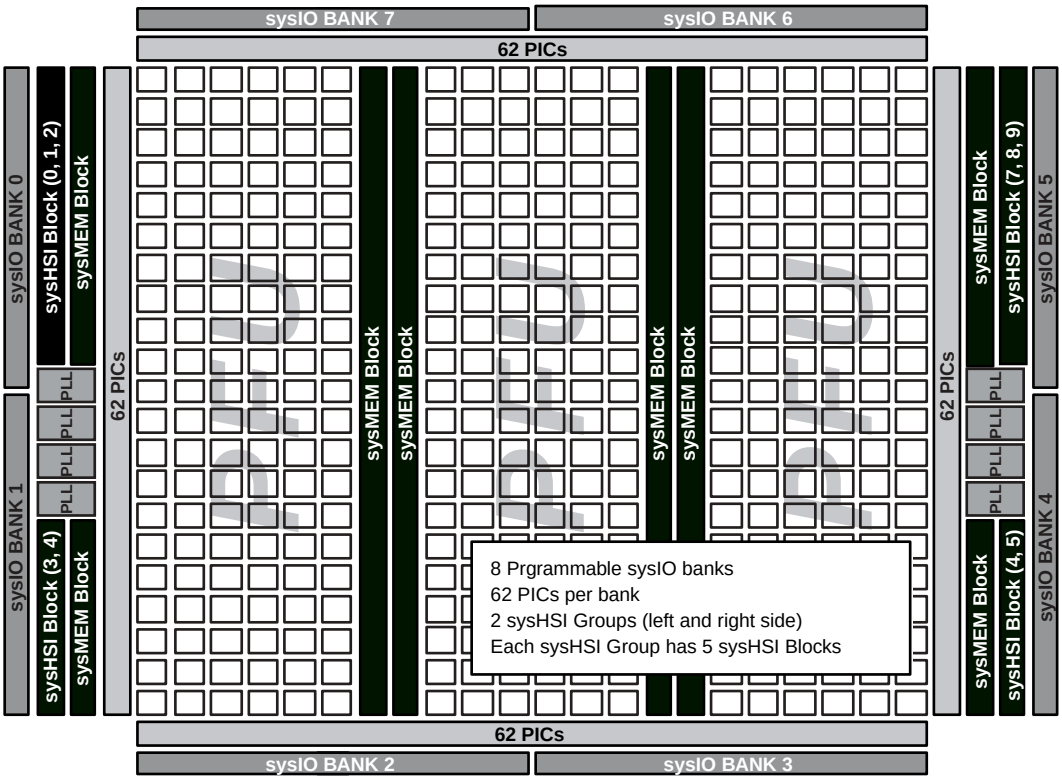
Synthesis tools such as Synplicity and Exemplar "black-box" the VHDL and Verilog instantiations and pass them through an EDIF netlist to the Lattice software. The Lattice software converts the "black-box" into the physical representation of the sysHSI within the device using the macros defined above. Verilog and VHDL pass the sysHSI attributes through parameters and generics, respectively.

Unlike other HDLs, ABEL requires special additions to support sysHSI functionality, the Lattice design tools provide direct support for ABEL and have been modified to support sysHSI functionality.

ispXPGA Family

The block diagram of LFX1200 is shown in Figure 8.

Figure 8. ispXPGA-1200 Block Diagram



sysMEM™ Embedded RAM (EBR) Usage as FIFO

spXPGA Family includes sysMEM Embedded Block RAM that can be programmed as a FIFO for synchronization. For macros available for the EBR, please refer to Lattice technical note number TN1028, ispXPGA sysMEM Memory Design and Usage Guidelines

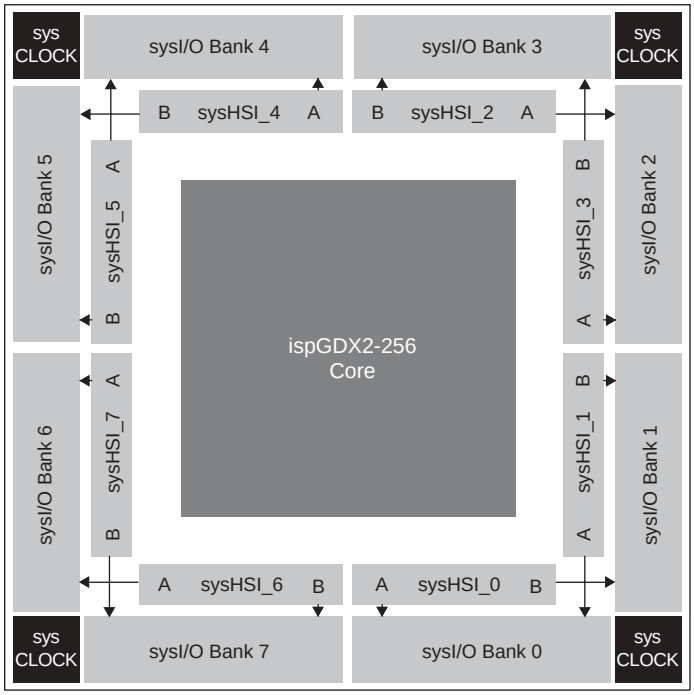
ispGDX2 Family

sysIO Banks and sysHSI Blocks

The ispGDX2 family devices are designed to minimize clock tree skew for high speed interface applications. The sysHSI sub-blocks, HSI_A and HSI_B are routed to nearest sysIO Bank.

The ispGDX2-256 has 8 sysHSI Blocks. Each sysHSI Block is divided to two SERDES blocks, HSI_A and HSI_B. Each SERDES block occupies 16 IO Cell Block in the sysIO Bank.

Figure 9. ispGDX2 sysIO Bank and sysHSI Block

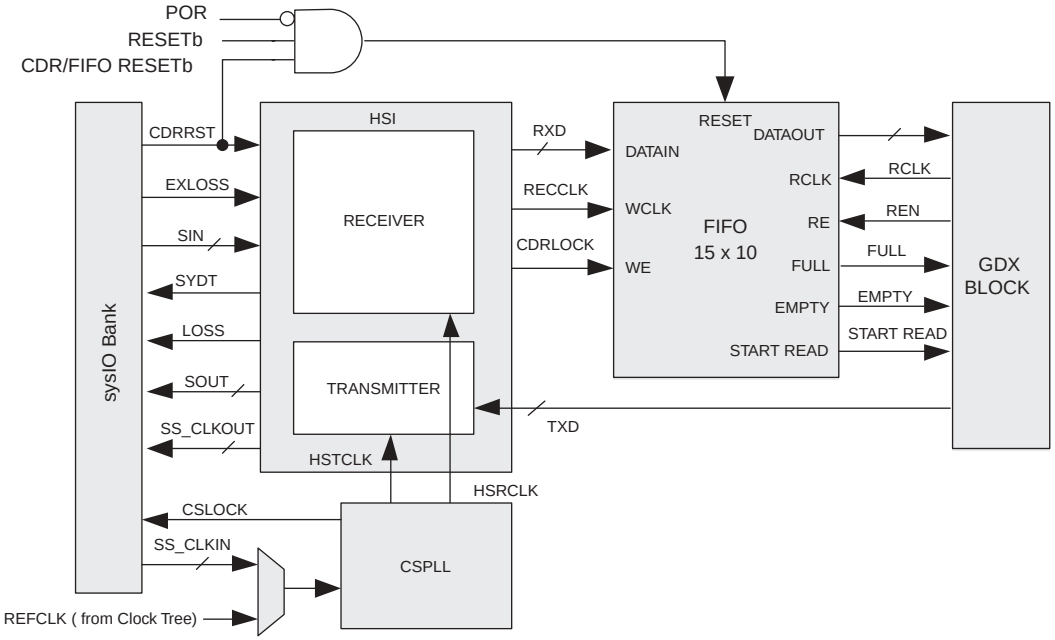


FIFO

sysHSI Block Interface with FIFO

The ispGDX2 Family includes dedicated FIFO for synchronization of recovered data. The FIFO is 15 x 10 and is intended to support CDR. The usage of FIFO is optional.

Figure 10. sysHSI Block interface with FIFO in ispGDX2



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